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INTREPID: Developing Power Efficient Analog Coherent Interconnects to Transform Data Center Networks

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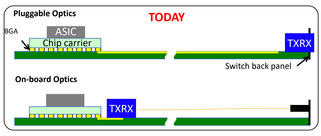
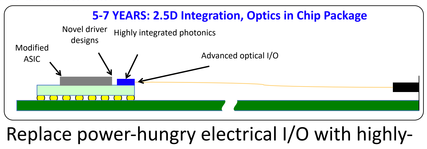
Integration of Photonic Interfaces into Chip Packages

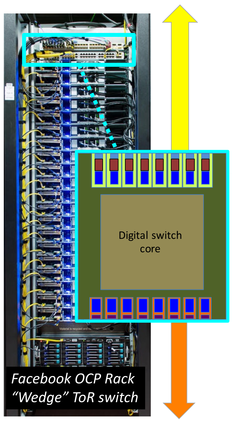
Conventional Packaging: Low integration level limits performance and efficiency



INTREPID: Energy-efficient coherent links for the datacenter

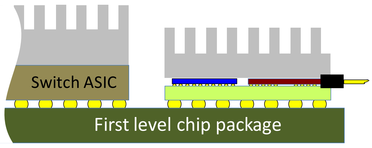


Replace power-hungry electrical I/O with highly-efficient photonics and use the power saved to expand switch radix



Analog Coherent WDM links

- Expanded link budgets enable photonic routing/switching
- Low power: no/very little DSP
- Target: 800Gb/s/fiber = 4λ@ 200Gb/s/λ (dual-pol QPSK, 50 Gbaud/s)



Multimode VCSEL links

- Server connections (30m)
- 50G → 100G

Analog Coherent Links: Maximizing Energy Efficiency

Direct Detection

Detected power ∝ (P_{laser} • A_{total})

P_{laser} = laser power, A_{total} = total link attenuation

- RX sensitivity sets energy efficiency
- Sensitivity degrades with datarate
  - Shrinking link budgets

Coherent Detection

Detected power ∝ $\sqrt{(P_{laser} \cdot A_{total}) \cdot P_{LO}}$

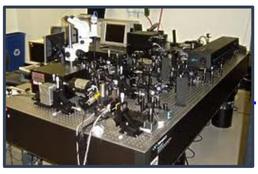
P_{LO} = Local Oscillator (LO) power

- ~20dB improvement in RX sensitivity
- Ability to compensate for insertion loss of optical routing/switching devices

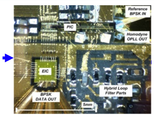
Optical Phase Locked Loop (OPLL) → Eliminating Power-Hungry DSP

OPLL locks phase and frequency of local oscillator allowing reception at low bit error-rate (BER) without forward error correction (FEC)

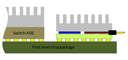
Typical OPLLs prior to 2000 — *Lab-scale*



Prior UCSB work — *Carrier-scale, single channel*



INTREPID — *Chip-scale, WDM*

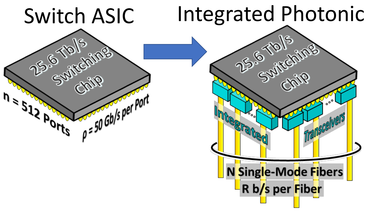


Photonic and Electronic Integration

<1000X size
<100X power

<10X size
<10X power

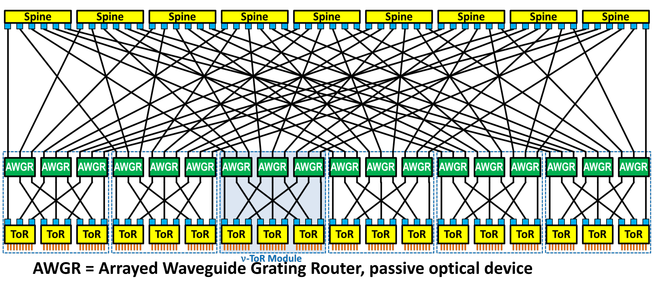
Integration AND Scalability



INTREPID Integration Target:
ν = 4 to 8 λ
r = 200 Gb/s per λ
R = 800 to 1,600 Gb/s per Fiber

INTREPID Coherent Integration		25.6 Tb/s Switching Chip n = 512 ports @ ρ = 50 Gb/s			L-Level Folded Clos			*Adding One AWGR Layer*	
# of λ's per Fiber	Bit Rate per λ (Gb/s)	Bit Rate per integrated Port or per Fiber (Gb/s)	# Chip Ports per Integrated Port	Number of Integrated Ports (RADIX)	Number of 50G Servers $2\,(R/\rho)\,(N/2)^L$			# of 50G Servers $2\,\nu\,(R/\rho)\,(N/2)^L$	
					L = 2	L = 3	L = 4	L = 2	L = 3
ν	r	R = ν r	R / ρ	N = n ρ/R					
1	100	100	2	256	65,536	*8.E+06*	*1.E+09*	65,536	*8.E+06*
2	100	200	4	128	32,768	2,097,152	*1.E+08*	65,536	*4.E+06*
4	100	400	8	64	16,384	524,288	*2.E+07*	65,536	2,097,152
4	200	800	16	32	8,192	131,072	2,097,152	32,768	524,288
8	200	1,600	32	16	4,096	32,768	262,144	32,768	262,144

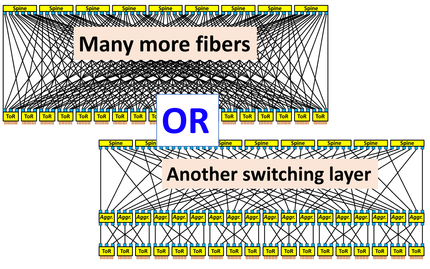
Scalability: added AWGR layer increases effective switch radix



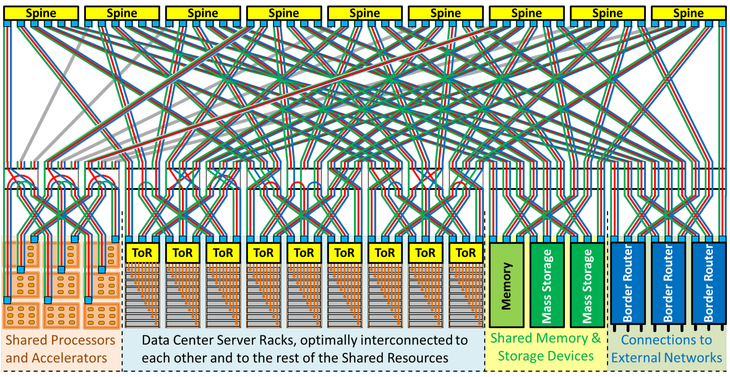
AWGR = Arrayed Waveguide Grating Router, passive optical device

Same number of servers with current technology

VS



Future: Optical-switch-based architecture



- **Disaggregation**
- **Configurability to match workload**
- **High utilization**
- **Improved energy efficiency**

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