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Compute Project

MiTAC Aowanda 1S1RU Server Sled

Rev 0.1

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1.2 Acknowledgements

The Contributors of this Specification would like to acknowledge the following companies for their feedback:

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2. OCP Tenets Compliance

1. Openness

The Aowanda 1U server sled compatible with Open Edge Chassis, Open Edge RMC, OCP 3.0 mezzanine card.

2. Efficiency

The server sled supporting 3rd Generation Intel Xeon Saleable processor. Increasing DDR4 memory speed and performance by the 8 channels of DDR4 slots design. Design with new generation of BMC chip controller; Aspeed AST2600 optimizes the performance and computing power.

3. Impact

The Aowanda 1U server sled supports PCIe Gen3 or PCIe Gen 4 EDSFF small form factor SSD. Enhance the storage density and thermal efficacy for improving NVMe performance.

4. Scale

Saleable for far edge outdoor, far edge, aggraded edge and regional workload.

3. Revision Table

Date	Revision #	Author	Description
2021/9/27	0.1	Michael Yeh/ Timothy Wang	Initial Release

4. Scope

This document defines technical specifications for the < MiTAC Aowanda 1S1RU Server Sled > used in Open Compute Project.

5. Overview

Aowanda Server Sled is a single socket design, half-width form factor MB and uses the Intel Whitley platform to fulfill the requirements based on OpenEdge Server v1.0. Aowanda has Model Names AD1S01 and AD1S02. Both SKUs are **1 RU** height and compatible w/ Aowanda **3U and 2U** chassis referenced Open edge chassis OCP contribution.

Aowanda Server is a compact, high-performance Server platform optimized for installation to edge sites, where facilities are limited in floor space, cooling capacity, and power feed capacity.

6. Rack Compatibility

MiTAC Aowanda 1S Server Sled is compatible w/ its Chassis SKU, including 3U and 2U referenced Open edge chassis OCP contribution. The Open edge chassis is compatible with standard 19” four-post racks (EIA-310).

7. Physical Specifications

7.1 MB Block Diagram and CPU/Memory Feature

- One Socket ICX /Ice Lake Processor w/ up to **185W**, Socket P+ w/ 4,189 pins, Whitely platform. The market family name is 3rd Gen. Xeon Scalable Processor
- PCH: C621A (Lewisburg)
- 8 Channels DDR4 per CPU @ 3200 MTS 1DPC
- PCIe G4 up to 64 lanes per CPU (bifurcation support: x16, x8, x4)

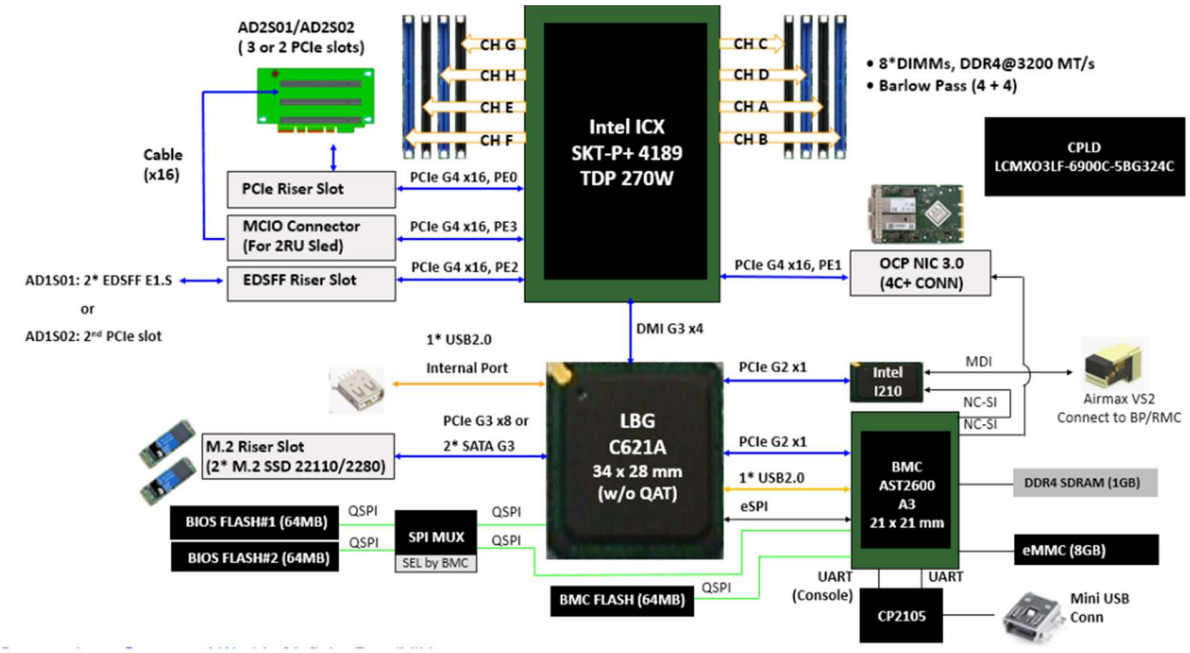


Figure 1 MiTAC Aowanda 1S Server Sled Block Diagram

7.2 MB Placement

Aowanda Server Sled is a half-width form factor MB and 12 stack-up layer w/ 1.93mm. Its Middle-loss materials are used for its PCB raw materials and targets at lower cost edge Server applications.

PCB:

- Dimension: 412.75 x 205.8, mm
- Stackup/thickness: 12 Layers / 1.93 mm

Figure 2 MiTAC Aowanda 1S Server Sled MB Placement

7.3 The Other Key Feature

- Ethernet controller I210AT
- BMC AST2600
- TPM 2.0 module
- On-Board Slots
  - ✓ 1RU Riser slot capable PCIe G4 x16 from CPU PE0
  - ✓ 1*EDSFF Riser slot capable PCIe G4 x16 from CPU PE2
  - ✓ 1*M.2 slot for carrying 2*M.2 SSDs (22110 or 2280) capable 2*PCIe G3 x4 from PCH HSIO
  - ✓ 1*MCIO connector (Amphenol Mini Cool Edge IO) cabling PCIe G4 x16 to 2RU Riser
  - ✓ 1* OCP NIC 3.0, small form factor, capable of the max 25W power budget
- Front panel LEDs/Buttons/Ports
  - ✓ Reset button
  - ✓ Power button integrated ID LED
  - ✓ Status LED
  - ✓ BMC heart-beat LED
  - ✓ 1*mini USB(Debug Purpose)
- Fans, 4*4056

- 1* USB Port(Debug Purpose Only and drop off after production)

7.4 OCP NIC 3.0

Aowanda Server Sled supports OCP NIC 3.0 card in small form factor and is capable of PCIe G4 x16 and 25W as the maximum power budget allowable. It's front side accessible.
Main Features:

- Small Form Factor (76 mm x 115 mm)
- PCIe G4 x16
- Maximum power budget: 25W
- NC-SI side-band management bus
- Front accessible

Figure 3 MiTAC Aowanda 1U Server supported OCP NIC 3.0 Card

7.5 SKUs and Daughter Cards

Aowanda 1RU Server Sled supports 5 small cards as below

- 1RU Riser: Supports One PCIe G4 x16 FHHL Card
- EDSFF Riser: Supports 2*E1.S Rulers by HSBP installed and carries PCIe G4 x16 lanes
- M.2 Riser: Supports 2*SSD in 22110 or 2280, PCIe G4 x16 lanes
- 1RU HSBP: Used to carry 2*Ruler and PCIe G4 x16 lanes
- 1RU Riser 2: Supports 1*Low Profile (or HHHL) PCIe card and carries PCIe G4 x8 lanes

	1RU Server-sled	1RU Server-sled
Model Name	AD1S01	AD1S02
1RU Riser	V	V
EDSFF Riser	V	X
1RU HSBP	V	X
M.2 Riser	V	V
1RU Riser2	X	V

Table 1: 1RU Server Sled Model Name and System Configurations

7.5.1 1RU Riser

It carries 16 lanes of PCIe G4 that came from the Processor, One PCIe x16 slot is on it. Except for PCIe G4 x16 lanes, there are still power rails (12V,3.3V, 3V3_AUX), Riser_ID, SMBus, and Present pin, routed around the slot.

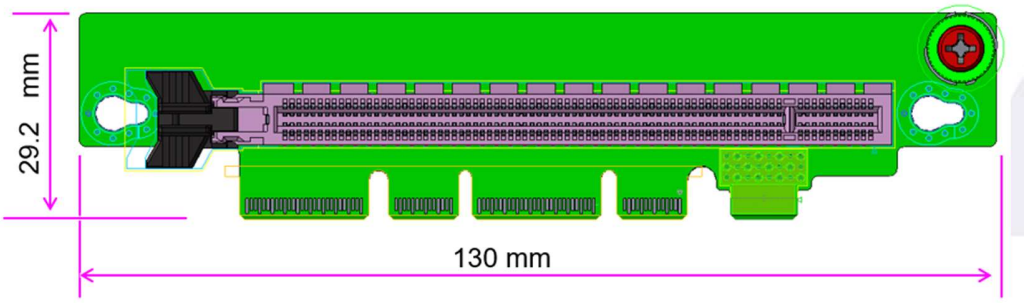


Figure 4 1RU Riser

7.5.2 1RU Riser 2

It supports one Low Profile PCIe card capable of PCIe G4 x8 that came from Processor and is different from EDSFF Riser designed to carry 2*Rulers by 1RU HSBP installed on EDSFF Riser .

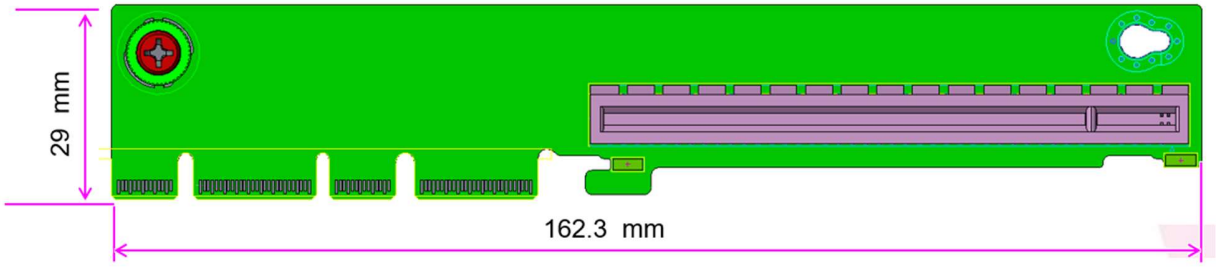


Figure 5 1RU Riser 2

7.5.3 EDSFF (Enterprise Datacenter Small Form Factor) Riser

EDSFF Riser supports 2*Rulers in E1.S Form Factor by 1RU HSBP installed on EDSFF Riser. There are PCIe G4 x16 lanes, SMBus, power rails (12V_stby, 3.3V_aux), Riser ID, Present signal, and EDSFF. Enable signal routed around the EDSFF slot.

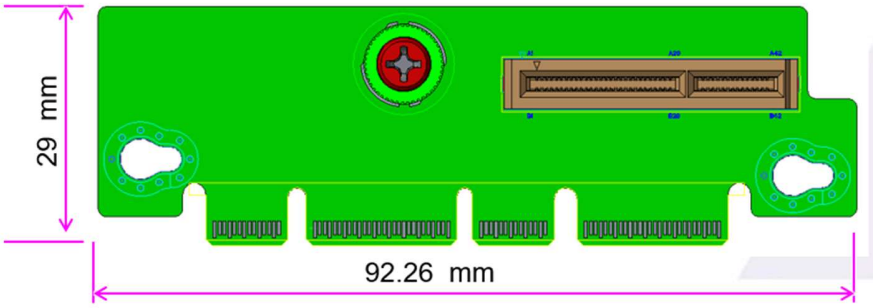


Figure 6 EDSFF Riser

7.5.4 1RU HSBP

It is designed to carry 2* Rulers and one CPLD controlled LED to indicate Rulers inactive or link status. It is installed on EDSFF Riser.
Features:

- ✓ PCIe G4 x16 from processor PE2 port
- ✓ SMBus, and Present signal
- ✓ Power rails (12V_stby, 3.3V_aux)
- ✓ One CPLD (LCMX02, Lattice) for LEDs management of Rulers

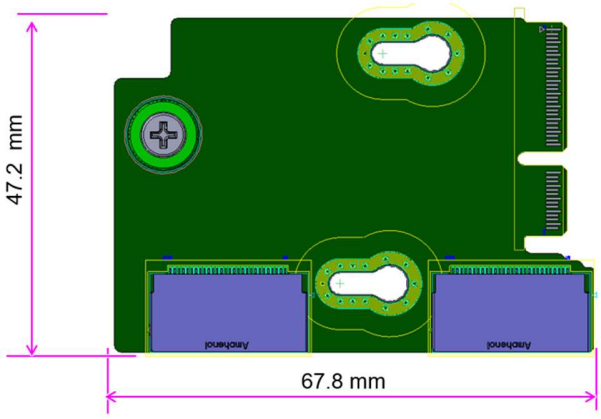


Figure 7 1RU HSBP

7.5.5 M.2 Riser

It supports 2* M.2 SSD w/ dimension of either 22110 or 2280. Thickness: 1.57mm

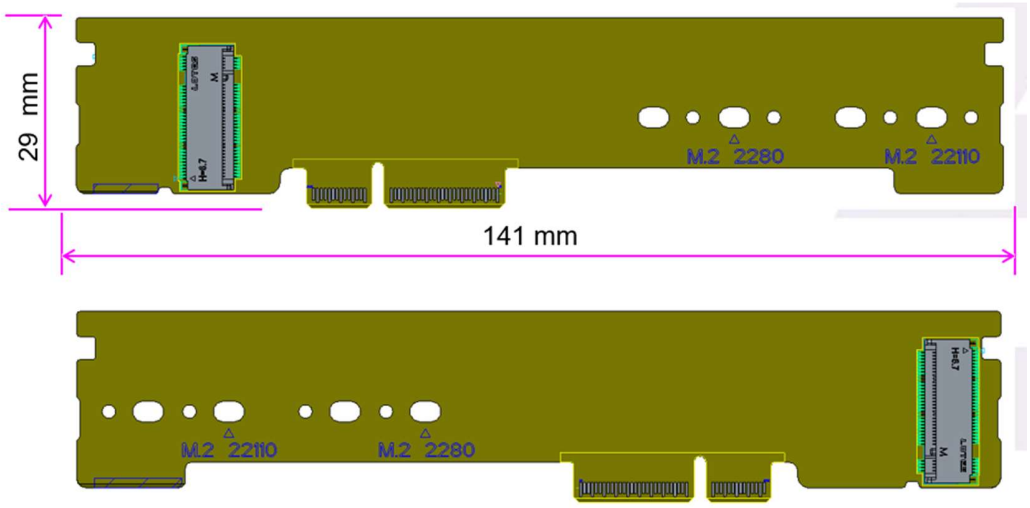
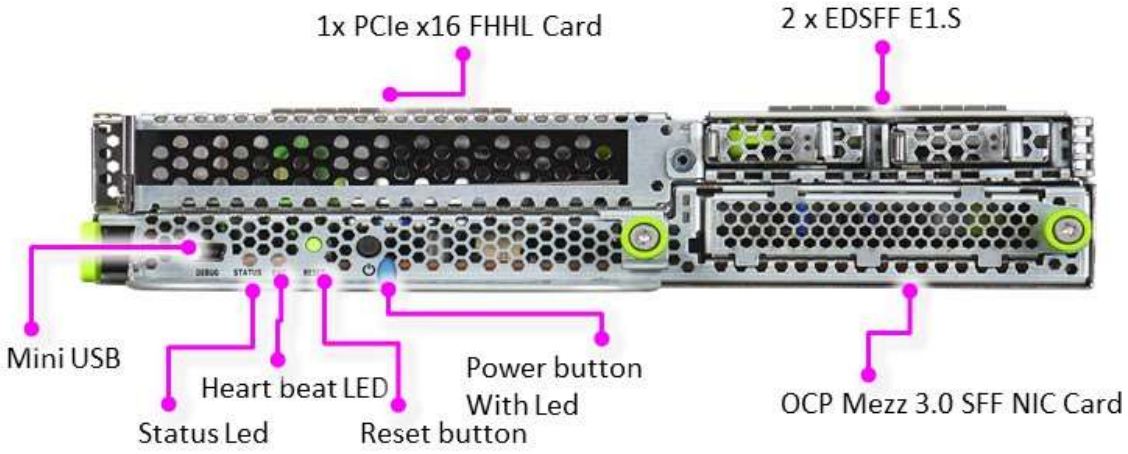


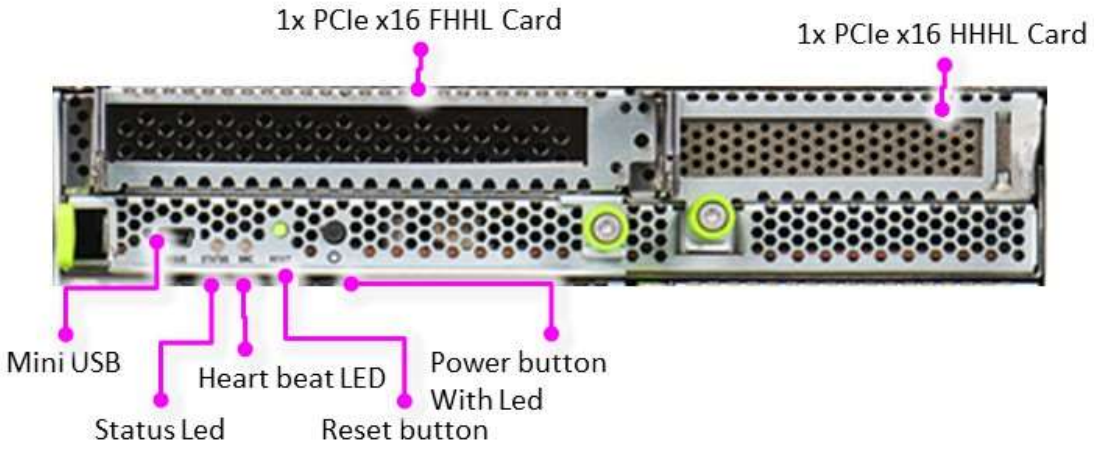
Figure 8 M.2 Riser

7.6 Front I/O on M/B

- Main Features:
  - ✓ Mini USB *1: Debug Purpose
  - ✓ Status LED: A tri-color LED (green/blue/amber) and is used to indicate System Healthy Status.
  - ✓ Heart-beat LED: A green LED. LED is turned on when BMC AST2600 is alive
  - ✓ Reset Button: Reset Server Sled
  - ✓ Power Button w/ LED: Power-on System. It is a blue LED and to identify the correspondent Server Sled. It is the only way to turn it on by keying in commands.



SKU: AD1S01



SKU: AD1S02

Figure 9 Front I/O Locations

8. Thermal Design Requirements

To meet Thermal Reliability requirements, the thermal and cooling solution should dissipate heat from the components when the system operating at its maximum thermal power. The thermal solution should be found by setting a high power target for initial design to avoid redesign of cooling solution; however, the final thermal solution of the system should be most optimized and energy-efficient under **Edge site** environmental conditions w/ the lowest capital and operating costs. The thermal solution should not allow any overheating issues for any components in the system.

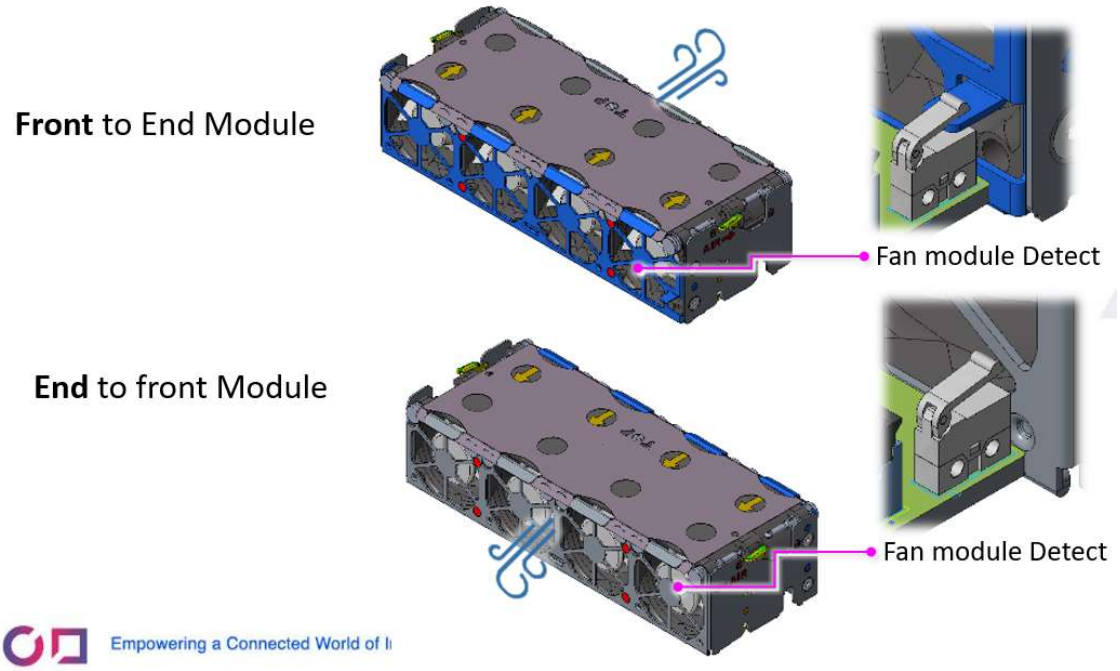
Cooling System: -5℃ ~ 45℃, including **One Fan Failure** Standard, Short Term 5℃ ~ 55℃ [GR-63-CORE]

SKUs:

- ✓ **AD1S01: Airflow Both Front-to-Rear or Rear-to-Front.**
- ✓ **AD1S02: Airflow Front-to-Rear.**

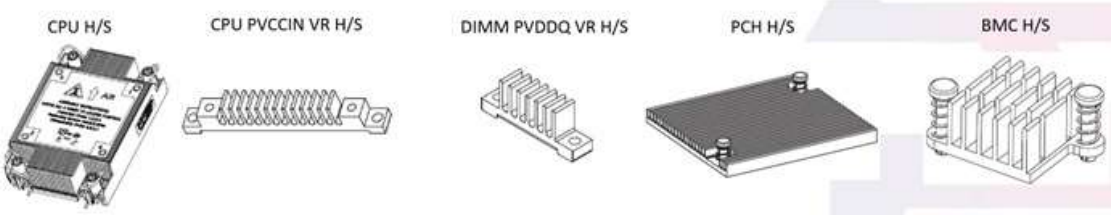
8.1 Thermal Components

4*4056 Dual Rotor Fan

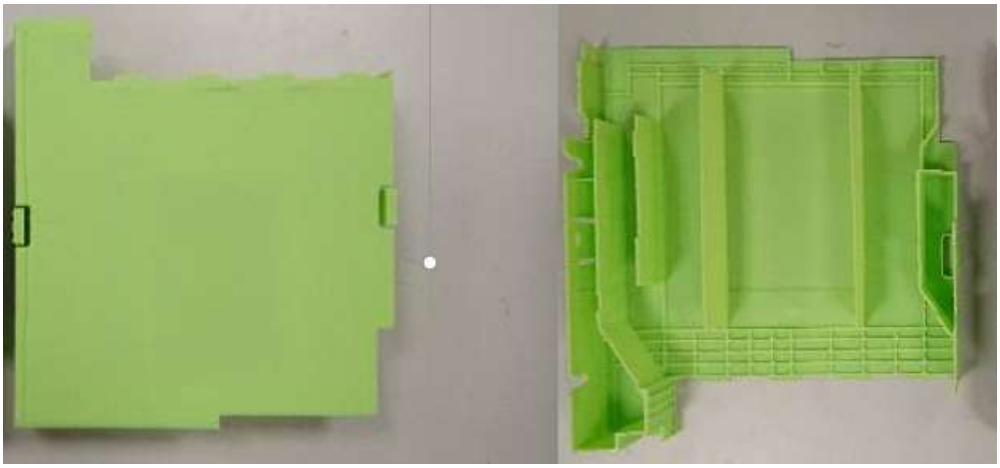


Aowanda 1S Server Heat Sinks

HS	Q'ty/ Sled	Mitac P/N	Fin Q'ty	Fin Thickness (mm)	Base Thickness (mm)	Materials
1U CPU H/S	1	343C51600014	46	0.3	4.5	Cu Block, Al base, Al Fin, 3x Pipe, TC-5026
CPU PVCCIN VR H/S	1	343C51600004	13	0.92	3.27	AL Extrusion, T-Flex HD-320, 2 screw
DIMM PVDDQ2 VR H/S	1	343C51600005	7	1	3.27	AL Extrusion, T-Flex HD-320, 2 screw
PCH H/S	1	343C51600008	27	1	1.8	AL Extrusion, 7762, 2 push-pin



Aowanda 1S Server Air Duct



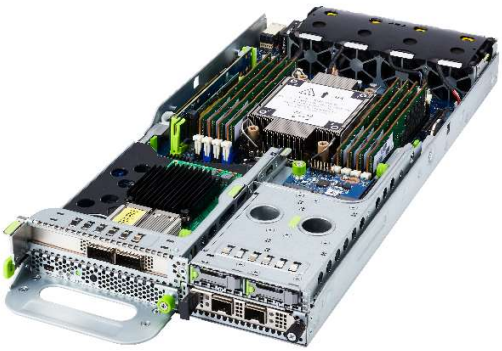
9. Rack Implementation

Static L Shelf Ready for EIA 19" 4 Post Rack

10. Mechanical

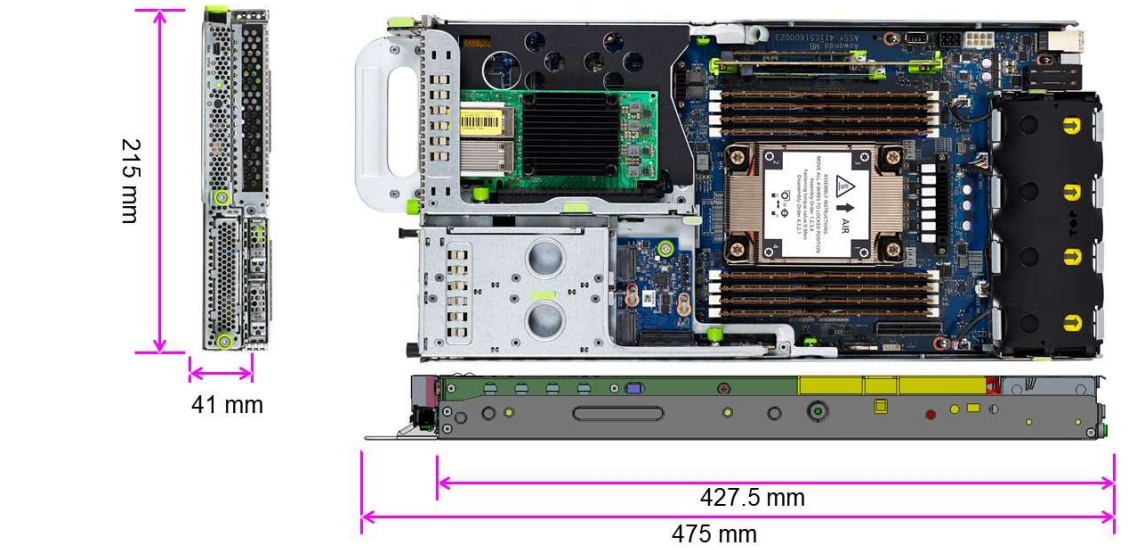
10.1 Aowanda 1S Server 1U SKUs

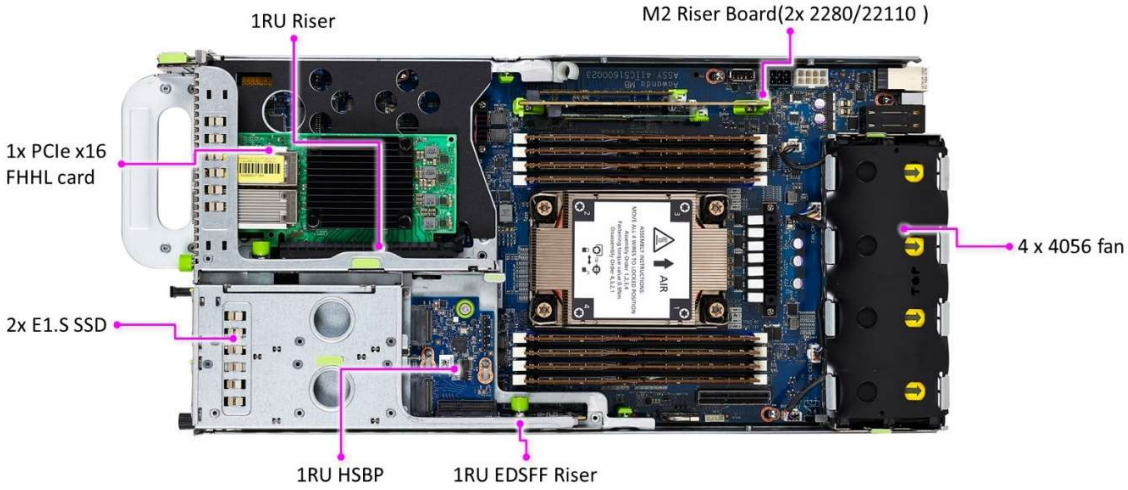
- Form Factor: 1RU Half-Width Open Edge Sled
- Dimensions: 215 x 475 x 41 mm(W x D x H)
- SKUs
  - ✓ **AD1S01:**
    - Two M.2 cards
    - One x16 FHHL PCIe card
    - Two E1.S SSD drives
    - One x16 OCP NIC 3.0 SFF card
  - ✓ **AD1S02:**
    - Two M.2 cards
    - Two x16 PCIe cards (1x FHHL+1x HHHL)



10.1.1 AD1S01

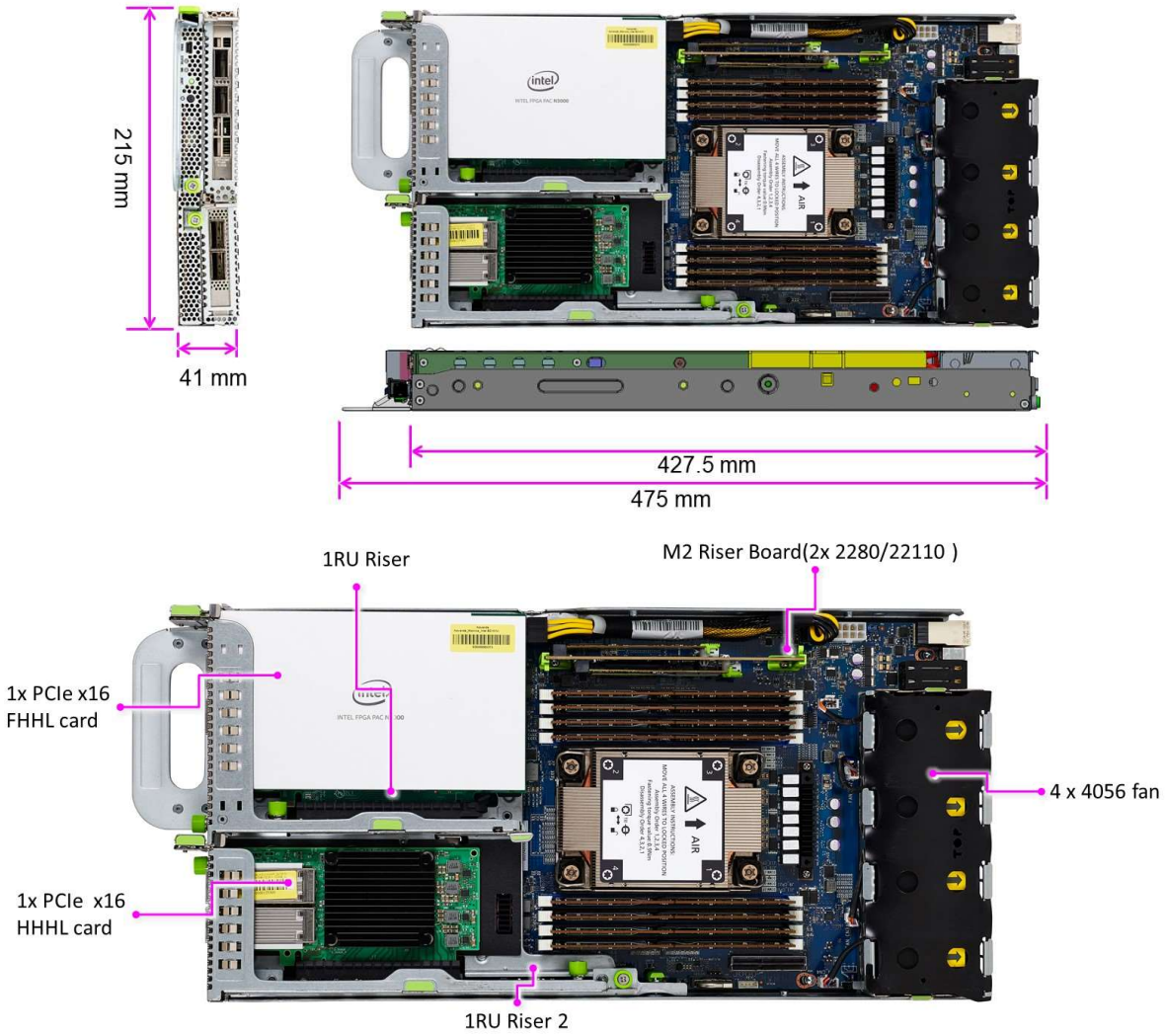
Dimension: 215(W) x 475(D) x 41(H)



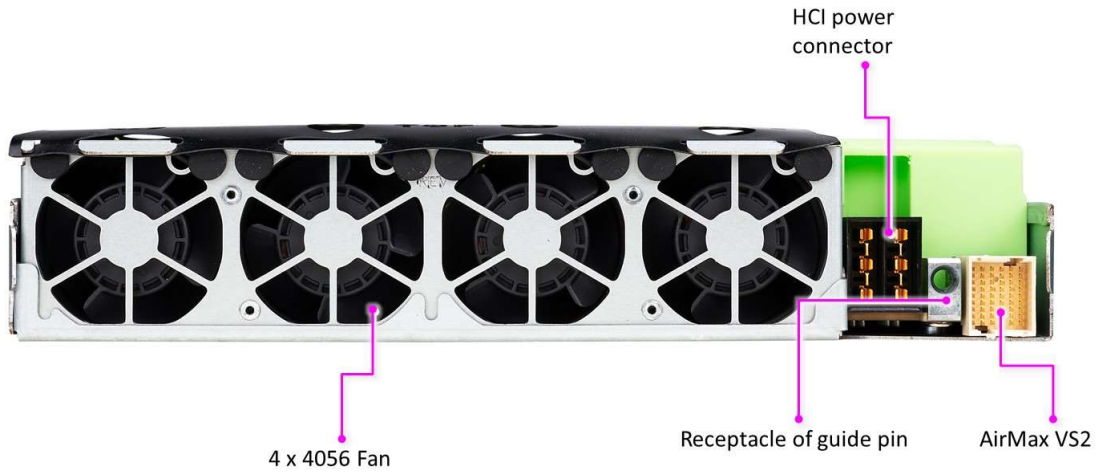


10.1.2 AD1S02

Dimension: 215(W) x 475(D) x 41(H)



10.2 Rear View of AS1S01 and AD1S02



11. Motherboard Power System

Except for PDB and PSU mentioned in Section 9.2 and 9.3 individually, Section 12 will focus on Power Rails in MB and corresponding PCBAs.

11.1 Power Rails – 3.3V (Main Power), and 12V (Aux Power)

Aowanda 1S Server MB offers **two** power rails **P3V3** and **P12V** to OCP NIC 3.0 card. P3V3 is the main power and P12V is Auxiliary power. These 2 power rails are controlled by CPLD, once OCP NIC 3.0 card is installed and detected by CPLD, then power rails will be enabled based on the associated situation of the OCP NIC 3.0 card.
it's +12V only routed to Server-sled MB. 12V goes into one HSC (Hot Swap Controller) Server-Sled then regulated to Power Rails demanded platform components and following as for reference to **SMBus, ALERT_N**

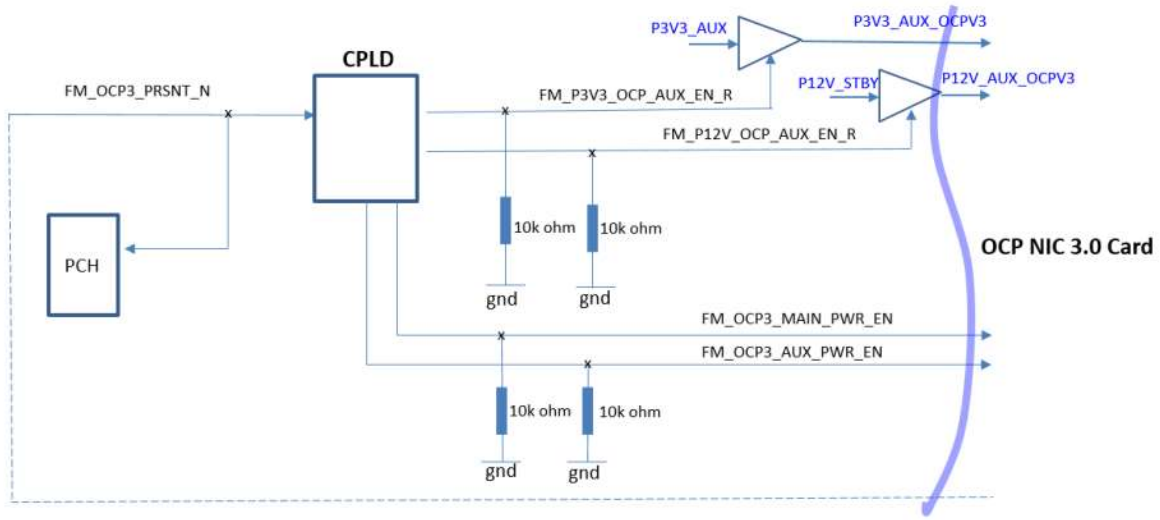


Figure 13 Power Rails for OCP NIC 3.0 Card: P3V3 (Main power) & P12V (AUX power)

11.2 Throttle

Aowanda 1S Server can enable Throttle. The following is an example to enable throttle once upon **ALERT_N** from PSUs asserted: "AND" circuit on RMC to allow no matter ALERT_N asserted from which PSU, then routed to PCH, triggers Throttle mechanism to degrade performance and meanwhile, records one event by BMC.

Certainly, there are a few ways to be able to trigger Throttle. Another example is when PCIe HBAs consume Power Budget over the planned budget. Or, when Aowanda server-sleds drawing current over the demands, Throttle is enabled as well.

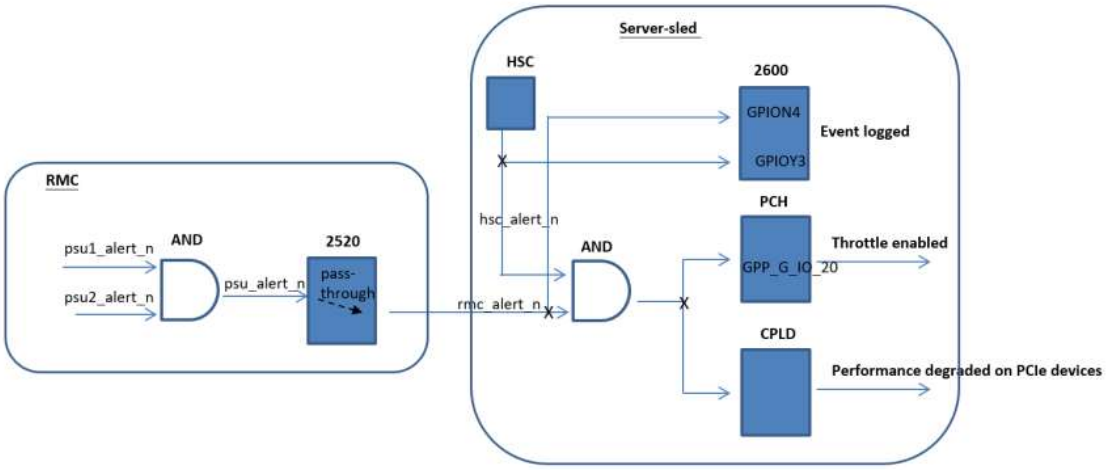


Figure 16: Throttle Trigger when ALERT_N from PSUs are asserted

12. Environmental and Regulations

UL/CE/FCC/ NEBS Level 3 Indoor: Will Follow **OpenEdge** and specific requirements of customers

13. Environmental Requirements

13.1 Operating Conditions

- -5℃ ~ 45℃, including **One Fan Failure** Standard
- Short Term 5℃ ~ 55℃ [GR-63-CORE]
- System Startup Temperature: 5 ℃
- Operating Humidity: 5 % to 95 % (OpenEdge Chassis OCP Contribution **v1.4**)
- Altitude: Up to 2,000m

14. Prescribed Materials

The disallowed components in the Aowanda 1S Server follow the European Union's Restriction of Hazardous Substances Directive (RoHS).

15. Software Support (recommended)

16.1. Software tools to validate the Hardware design

Please list any software tools used to validate the hardware design. The tools could be related to:

- Test and Validation using virtual simulation
- Design decision based on digital models
- Proof of manufacturability with 3-D tools

16. System Firmware

16.1 BIOS AMI UEFI BIOS, 64 MB SPI Flash

- A BIOS image resides in the SPI flash part which is along with other components, such as Intel Management Engine FW, platform descriptor, device expansion region, etc. The flash consists of several regions for storing these components.
- BIOS shall provide proper utilities to support flash image update operations. In update progress, these utilities shall support the most frequently used scenarios listed below.
  - ✓ Users can export the current BIOS settings to a file.

- ✓ Users can override BIOS SETUP settings with predefined configurations.
- ✓ Update partial image with the user-specified region of flash.
- ✓ Retain the current setting while updating the new BIOS.
- ✓ BIOS update utility shall support Command Line Interface (CLI) mode.

16.1.1 BIOS Main Features

- Information Displayed during POST Time
- BIOS Hotkeys
- Remote Combination Hotkeys
- BIOS POST Code
- BMC FRB2 Watch Dog Timer
- Altitude
- Start of POST and End of POST Information
- Manufacture Mode

- Redfish Support
- WHEA ID
- Endless Boot Support
- iSCSI Boot Support
- Intel RSD Support
- TCG Support
- Configuration of PXE and iSCSI
- Security Frozen Mode
- Virtualization Configuration
- Synchronize FRU to SMBIOS
- BIOS Image Update during POST
- BIOS SETUP Configuration Version

16.1.2 SMBIOS Support

System Management BIOS (SMBIOS) addresses how MB presents management information about its product in a standard format by extending the BIOS interface. The information is intended to allow generic instrumentation to deliver this data to management applications. BIOS shall support SMBIOS 3.3 or above and be filled in defined types and columns. Followings are a brief list of supported tables.

- ✓ Type 0: BIOS Information

- ✓ Type 1: System Information
- ✓ Type 2: Baseboard Information
- ✓ Type 3: System Enclosure or Chassis
- ✓ Type 4: Processor Information
- ✓ Type 7: Cache Information
- ✓ Type 9: System Slots
- ✓ Type 11: OEM Strings
- ✓ Type 16: Physical Memory Array
- ✓ Type 17: Memory Device
- ✓ Type 19: Memory Array Mapped Address
- ✓ Type 38: IPMI Device Information
- ✓ Type 41: On Board Devices Extended Information
- ✓ Type 127: End-of-Table
- ✓ *Type 190 : NIC Information
- ✓ *Type 192 : PCIe Information
- ✓ *Type 193 : Processor CPUID Information
- ✓ *Type 194 : Storage Device Information
- ✓ *Type 195 : Trusted Platform Module Information
- ✓ *Type 196 : Intel Trusted Execution Technology Information
- ✓ *Type 197 : Memory Device Extended Information
- ✓ *Type 198 : FPGA Information
- ✓ *Type 200 : SMBIOS Physical Device Mapping Information

  * Required when supporting Intel RSD

16.1.3 Remote Connection

BIOS supports the Console Redirection feature. When it is enabled, the system can be operated w/o a keyboard or monitor attached to the host system and operated entirely from a remote console. It's implied that any other text-based utilities can be accessed through console redirection. The settings of local physical COM port and SOL default are enabled for both ports. When users try to change different console baud rate settings, BIOS will not have a chance to synchronize this setting to RC RMT and debug mode phase. So it might be caused to output garbled text on console interface.

16.1.4 Error Handling

- ✓ Memory Correctable ECC Threshold Setting
- ✓ ECC Error Event Log Threshold
- ✓ Uncorrectable ECC Error
- ✓ BIOS POST Code

16.1.5 Power Management

- ✓ ACPI Power State
- ✓ Wake States Support

16.1.6 Interaction between BIOS and BMC

16.1.6.1 Pre-Boot BMC Action

BMC controls power supplies in a system but DC power on and off controlled policies are set primarily through BIOS setup. Before the BIOS POST activity begins, the BMC has responsibility for sequencing power from an AC-present or AC-absent state to fully DC-on w/ the BIOS boot process started.
When AC power is not present due to a power failure happened, the BMC follows the “Power Restore Policy” that had been established before the power failure condition.

16.1.6.2 Early of POST Stage

BMC will enable a **Watch Dog Timer** before BIOS starts to run. At the beginning of POST, BIOS issues a **START SIGNAL** to BMC via a **GPIO pin**. Then, BMC Watch Dog Timer was enabled and set the timeout value was **6 minutes**. If it expired, BMC assumed that BIOS POST is hung and Reset the system.
In this early stage, BMC and BIOS synchronize w/ each other on power policies. BMC will maintain Power Restore Policy which is synchronized from BIOS Setup Menu that the user will change the settings.
BMC will retrieve system time via reading PCH RTC time. Therefore, BIOS shall not do time synchronization with BMC.

16.1.6.3 During of POST Stage

BIOS records errors into the System Event Log through interacting with BMC. BMC also snoops the POST Progress Codes, Port 80 codes included RC (Reference Code), and AMI POST Codes.

16.1.6.4 End of POST Stage

At the end of POST, BIOS will send a notification to BMC via a **GPIO** pin.

16.1.6.5 BMC LAN Configuration in BIOS Setup Menu

BIOS allows for setting BMC LAN Configuration parameters included IPv4 and IPv6 addressing options via IPMI commands.

16.1.7 Bootable Device Order

16.1.7.1 Bootable Device Category

BIOS must support Preboot eXecution Environment (PXE) boot capability in both IPv4 and IPv6 environments, and boot from SATA, SAS, and USB interface. BIOS should also provide boot selection items in the setup menu and support a hotkey to prompt a menu for user selection during BIOS POST time. Built-In shell shall be removed.

The supported bootable device including but was not limited

- ✓ USB Devices
- ✓ SATA Devices
- ✓ LAN Devices
- ✓ NVMe(Added AMI NVMe supported module)

16.1.7.2 Boot Order on UEFI Mode

Default Boot Order is

- ✓ Onboard SATA/PCIe M.2
- ✓ PCIe NIC Cards with IPv6
- ✓ PCIe NIC Cards with IPv4
- ✓ Onboard LAN with IPv6
- ✓ Onboard LAN with IPv4
- ✓ USB Optical Disc Drives
- ✓ USB Hard Disk Drives
- ✓ Other bootable devices

If there is no bootable device found, BIOS should keep the loop searching for a bootable device. Furthermore, boot mode and boot order shall be displayed and changed from BMC with OEM command.

16.1.7.3 A prefix of Network Boot Option Name on UEFI Mode

In the BIOS Setup menu, Network devices could be presented to bootable media via PXE or HTTP mechanism. For easier to distinguish the boot option name, BIOS shall add the Prefix to each presented Network boot option in the below format.

UEFI: [PXE | HTTPS] [IP4 | IP6] [Device Name] [MAC Address]
E.g. UEFI: PXE IP6 Intel(R) I210 Gigabit Network Connection 00224DD5D3DD

16.1.8 BIOS Security

BIOS Setup Menu will contain a Security Page for a user to set a password. It is used to protect unexpected authorization to access the BIOS setup menu and change the settings.

Password strength is designed by the BIOS vendor. The minimum length is **8** characters and the maximum length is **20** characters1. The password would be case-sensitive and cleared when **CMOS clear jumper** is asserted or the **CMOS battery** is removed.

An authorized user could set a proper password before delivering and the security grade was also divided into two different kinds of levels, one is the administrator and the other is user level. A different level could present different kinds of BIOS setup items. It depends on customer requests.

16.2 BMC Aspeed AST2600

BMC FW implements IPMI 2.0 based on AST2600 service processor. It performs all the BMC management tasks defined by IPMI 2.0 and, as a Service Processor, allows for remote monitoring using **Serial Over LAN**.

16.2.1 H/W Component

Component	Size	Usage
Aspeed AST2600	NA	It's a vastly integrated SOC device playing as a service processor to support various functions required for highly manageable server platforms.
DDR4 SDRAM	512MB	BMC memory
SPI flash	64MB	BMC Flash part includes BMC FW, user configuration, SEL and SDR.
EEPROM	128KB	FRU information

16.2.2 BMC Main Features

Feature		Description
IPMI 2.0 Standard Features	System Interface support	• KCS • LAN(RMCP/RMCP+)
	Text Console Redirection: SOL	• Support in IPMI stack for SOL to remotely access BIOS and text console before OS booting.
	IPMI 2.0 based Management	• BMC stack with a full IPMI 2.0 implementation • Optional commands supported(refer to section 4.1.1) • OEM commands supported(refer to section 4.1.2 and section 5)
	System Management	• System health monitoring. • System Power management • Fan speed monitor and control
	Event Log and Alerting	• Read Log events • Sensor readings • SNMP traps
	Remote Server Power Control	• Server's power status report • Support for remotely power-cycle, power-down, power-up, reset the server
	Watchdog Timer Support	• Watchdog function that can generate interrupt or reset after zero count down
	Sophisticated User Management	• IPMI based user management • Multiple user permission level • Extended security algorithms and cipher suites support
OEM features	Management Network Interface	• BMC should has Shared-NIC uses RMII/NCSI interface for Out-of-Band access.
	Port 80 POST	• BMC to support port 80 POST code display to drive 8 bit HEX GPIO and SOL • BMC should have access to POST code and record up to 256 POST codes.
	FSC in BMC (Not ready)	• BMC should support FSC in both PID and step mode. BMC should support both In-Band and Out-of-Band FSC configuration update; updates should take effect immediately without reboot required. BMC should support FAN boost during fan failure. • Default fan PWM setting is 100% when power on by HW.
	Control Power and System Identification LED (Power LED no define)	•
	YAFU BMC/BIOS remote update(Not ready)	•
	BMC web GUI	•

16.2.3 BMC Messaging Interface

BMC Messaging interfaces complies w/ IPMI 2.0 Specification. The following interfaces are supported.

- ✓ Keyboard Controller Style (KCS) Host Interface
- ✓ LAN Interface
- ✓ IPMI Serial/Modem Interface

16.2.4 Text Console Redirection – SOL (Serial over LAN)

Aowanda BMC FW provides support for text console redirection (SOL) to remotely access BIOS setup or text consoles that are available on the serial console of host system.
FW includes support for IPMI based SOL where the standard IPMI client like IPMITOOL that used to establish a SOL session w/ a service processor.
SOL default baud rate is setup by BMC flash part as 115200. BMC and uEFI will synch at the System booting POST stage.

16.2.5 Commands Support

Aowanda BMC FW provides a fully-compliant IPMI 2.0 based management of Service processor. All the mandatory requirements and commands in IPMI 2.0 are supported

16.2.6 OEM Command Support

Except for Standard and optional commands, Aowanda BMC provides the system specific OEM commands that dedicated for Aowanda system.

16.2.7 Event Logging and Alerting

All System events are logged in an internal 64K bytes flash. However, Aowanda BMC does not support any alert mechanism based on mfg per-configured Alert Policy.

16.2.8 Chassis and Power Control

This section describes chassis control mechanism of Aowanda 1S Server Sled. The related chassis commands are specified in chapter 28, IPMI v2.0.

16.2.8.1 Chassis Capabilities

- ✓ Provides Monitoring Interrupt(NMI)
- ✓ Chassis provides intrusion sensor

16.2.8.2 Chassis Control

BMC must have ability to perform System Power On/Off and Reset functions. These functions will be controlled externally through IPMI chassis commands that described in IPMIv2.0 specification. It includes Get chassis capabilities, Get chassis status, and Chassis control, these kind of commands are mandatory IPMI commands and must be implemented.

- ✓ Power Down
- ✓ Power Up
- ✓ Power Cycle
- ✓ Hard Reset

16.2.9 Port 80 POST

Aowanda BMC supports Port 80 POST code display to drive 8 bit HEX GPIO from debug header described. BMC POST function would be ready before System BIOS starts to send 1st POST code to port 80

16.2.10 LED Control by BMC

16.2.10.1 BMC Heartbeat LED

BMC heartbeat LED will be blinking while BMC is alive. Otherwise, it must be deactivated while BMC's firmware is out of working.2

16.2.10.2 Power / ID (Identify) LED (Color: Blue)

According to Aowanda HW design, ID LED is combined w/ Power Button/LED

State	Description
On	SLED DC on (no IPMI identify command action)
Off	SLED DC off (no IPMI identify command action)
Blinking	IPMI chassis identify command running

16.2.10.3 State LED (Color: Red)

State	Description
Off	Normal operation
Blinking	If any threshold sensor has critical/warning alarm

16.2.11 BMC FW Update

Aowanda BMC supports i**n-band** and **out-of-band** flashing of the BMC FW via tools as below.

- ✓ Yafuflash via local USB or remote host via network for Linux (CentOS 6.8/7.3 64-bit).
- ✓ Socflash: provide by Aspeed. Linux (CentOS 6.8/7.3 64-bit) and DOS

16.2.12 BMC Time Sync.

- ✓ BMC Initialization: BMC auto sync.s System RTC via PCH SMBus Command.
- ✓ During POST:
  Step1. BIOS send “IPMI Get SEL Time UTC Offset” command
  Step2. BIOS send “IPMI Set SEL Time” command to BMC.

16.2.13 BMC&CPLD Control Throttle when System Power is over 550W

Due to Aowanda Chassis Total Power Limitation (2000W), there is concern that one Aownada 1S Server Sled power if over 550W. So to add feature that setting Apwanda 1S Server Sled throttled behavior at 550W and then back to normal at 450W for protection.

- ✓ SLED power throttling while 548.6W:

While HSC Input Power sensor reading reaches 548.6W, BMC triggers UC assertion SEL as well as set SGPIO76 pin state high to inform CPLD on throttling.

- ✓ SLED power recovered from throttling while 449.8W:

While HSC Input Power sensor reading lower than 449.8W, BMC triggers UC de-assertion SEL as well as set SGPIO76 pin state low to inform CPLD recovery from throttling.

16.3 CPLD (Lattice LCMX03LF-6900C)

Main CPLD Features in Aowanda 1S Server Sled

- ➢ CPLD detects AC PSU failure, asserts ADR_TRIGGER signal to PCH
- ➢ Aowanda 1S Server Sled has two power rails P3V3 and P12V connected to OCP NIC 3.0 card. P3V3 is main power and P12V is Auxiliary power. These 2 power rails are controlled by CPLD and once OCP NIC 3.0 card installed and detected by CPLD, then power rails will be enabled based on the associated situation of OCP NIC 3.0 card.
- ➢ 1RU HSBP is designed to carry 2* Rulers and One CPLD used to control LEDs to indicate Rulers in active or link status.