OPEN

Compute Project

Inspur Server

Project San Jose

Rev 1.01

Author: Inspur San Jose Team

1. Revision History

Version	Date	Description	Name
0.10	1/12/2017	Initial Release	Kevin Liu
0.11	1/25/2017	Update	Kevin Liu
0.12	8/1/2017	Updated	David Chamberlain
1.00	8/15/2017	Update	Kevin Liu
1.01	8/29/2017	Update links	David Chamberlain

Note: Because the product version upgrade or other reasons, the contents of this document will not be updated on a regular basis. Unless otherwise agreed, this document used only as a guide, in this document, all statements, information and advice does not constitute any express or implied guarantees.

■ License

Specification is assumed by the Specification implementer and user. IN NO EVENT WILL ANY PARTY BE LIABLE TO ANY OTHER PARTY FOR LOST PROFITS OR ANY FORM OF INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES OF ANY CHARACTER FROM ANY CAUSES OF ACTION OF ANY KIND WITH RESPECT TO THIS SPECIFICATION OR ITS GOVERNING AGREEMENT, WHETHER BASED ON BREACH OF CONTRACT, TORT (INCLUDING NEGLIGENCE), OR OTHERWISE, AND WHETHER OR NOT THE OTHER PARTY HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGE.

2. Scope

This document defines the technical specification for San Jose Motherboard and chassis used in Open Compute Project Open Rack V2.

3. Contents

4. Overview

4.1 Product Overview

San Jose is a completely independent research and development of server products. Based on Intel® Skylake CPU architecture, using Lewisburg chipset. Support two mainstream Intel Xeon Skylake series processor. Support 16 DIMMs DDR4 memory, the biggest support to 2666 MHZ. Supports a 3.5 -inch SATA disk or 2 blocks of 2.5 -inch NVMe hard disk, and supports SATA/PCIE M. 2 on motherboard. PCI Express support expansion slot X24 + X8. Supports OCP

MEZZ connecter A, B and C, extended SATA * 9 or SATA * 5 and second block PCIE M. 2 disk. Structure, storage, PCI extension, power supply, fan and other parts modular design. Centralized power supply design, to realize saving energy and reducing consumption.

4.2 Product standard

CPU	
CPU type	Intel® Skylake series processor (the highest support two 165W CPU)
Connecter	Two Socket-P slot
Chipset	
Chipset type	PCH LBG-2 or LBG-T
RAM	
RAM type	DDR4 ECC RDIMM/LRDIMM
RAM slot quantity	16
RAM total capacity	Total capacity 2048GB（single 128GB）
I/O Connecter	
USB	USB 3.0*2 preposition, one USB 3.0 for debug
VGA	Mini VGA preposition
Network card	
Network card controller	BMC chipset on Motherboard. Support OCP MEZZ connecter A, B and C.
Manager chipset	
Manager chipset	Integrated one independent 1000 Mbps network interface, specifically for remote management of IPMI.
PCI Express slot	● The motherboard with PCI Express 3.0 x24 slot + x8 slot ● Riser card support one full high full length standard card on crosswise.

	● Support one 80mm SATA M.2 or 110mm PCIE M.2 on side.
HDD	
HDD type	Support one 3.5 inch SATA HDD
	Support two 2.5 inch NVMe SSD or 2.5 inch SSD
Power supply	
PSU spec	1. The Rack uses two power shelf, every shelf using 3 + 3 redundancy mode PSU, every PSU support 2.1kw, and total 12.6kw in the Rack. 2. The Rack uses two power shelf, every shelf using two 3.3kw PSU and one BBU, and total support 13.2kw.
Input power	1. 125V/208VAC 3-Phase Input 2. 277V/480VAC 3-Phase Input

5 Physical Specifications

5.1 Block Diagram

Figure 5-1 illustrates the functional block diagram of the Motherboard.

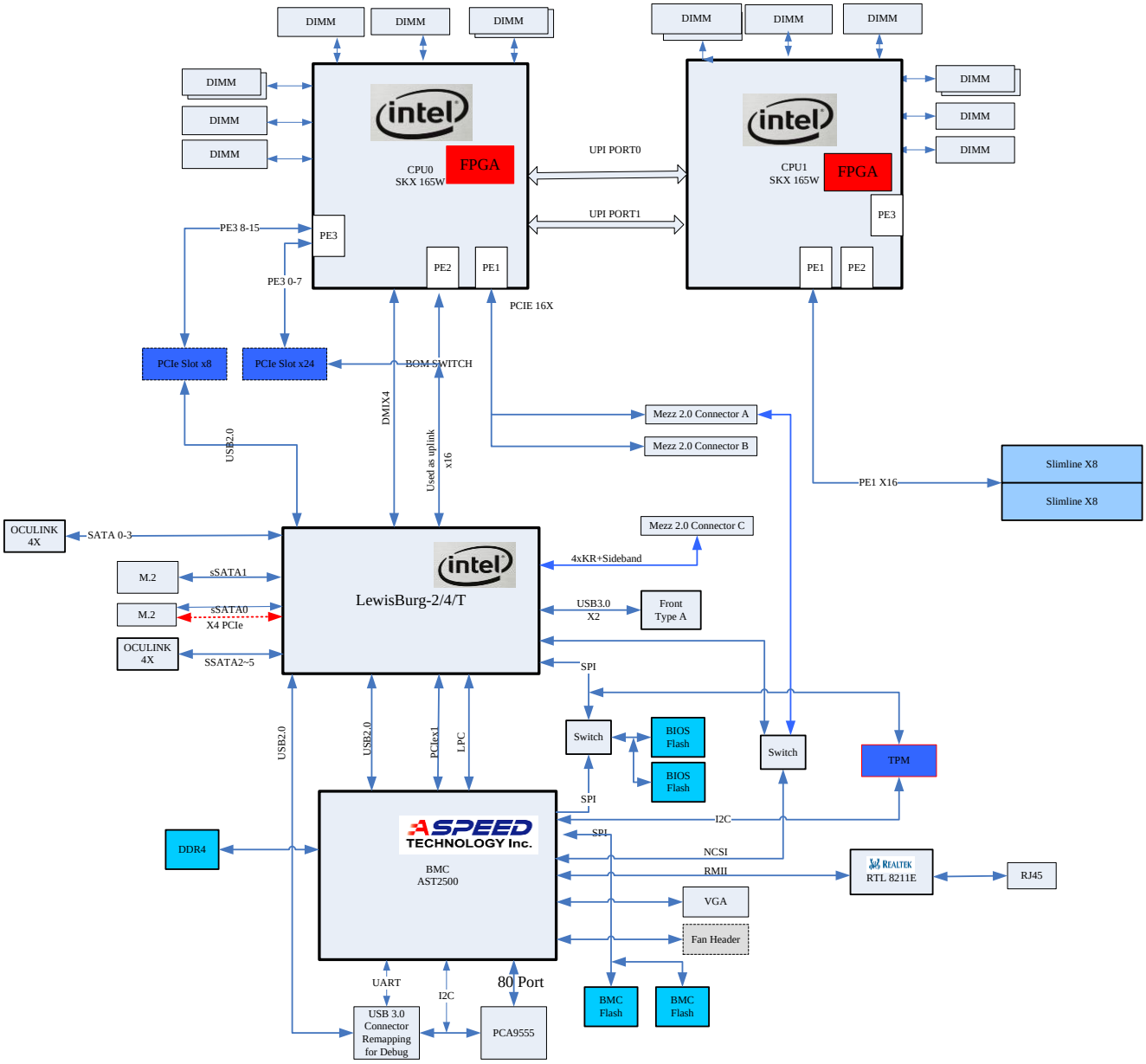
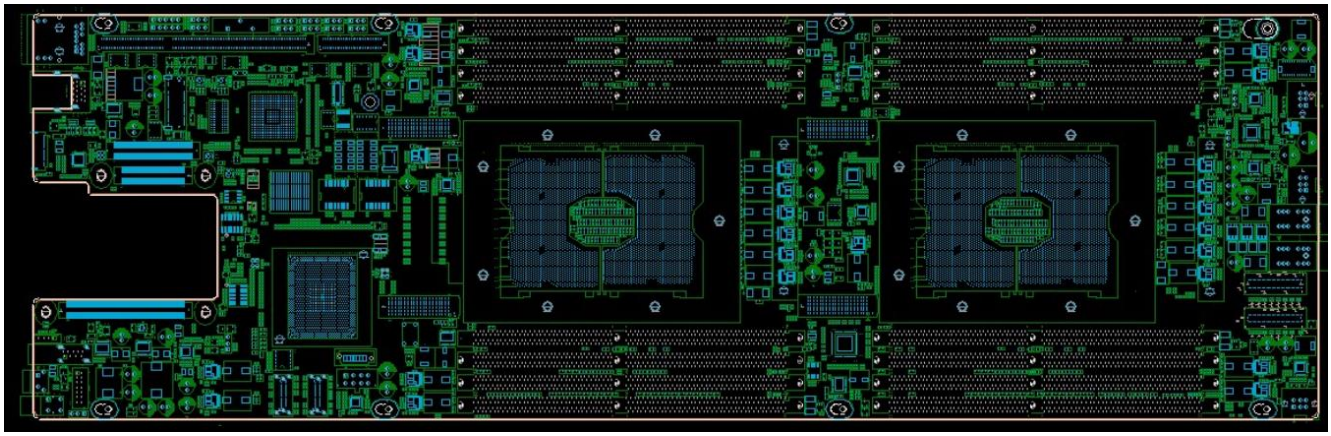


Figure 5-1

5.2 Placement and Form Factor

Board form factor is 6.5 inch by 20.6 inch (6.5”x20.6”). And Figure 5-2 illustrates board placement. The placement is meant to show key components ’relative positions, while exact dimension and position information would be exchanged by DXF format for layout and 3D model for mechanical.



Placement

5.3 CPU and Memory

5.3.1 CPU

The motherboard supports all Intel® Skylake processors with TDP up to 165W.

- Support two Skylake processors up to 165W TDP.
- Two full-width Intel UPI links up to 10.4 GT/s/direction for Skylake processor.
- Up to 28 cores per CPU (up to 56 threads with Hyper-Threading Technology).
- Single Processor mode is supported
- FPGA SKU CPU up to 165W is supported on both CPU0 and CPU1 with BOM option with MCP VRMs for both CPU sockets

5.3.2 DIMM

The motherboard has DIMM subsystem designed as below:

- DDR4 direct attach memory support on CPU0 and CPU1.
- 6x channels DDR4 registered memory interface on each CPU
- 2x DDR4 slots on Chanel A and D, other support 1x DDR4 slot (total 16x DIMM)
- Support DDR4 speeds up to 2666
- Support RDIMM, LRDIMM DDP, LRDIMM 3DS TSV-4H
- Support SR, DR, QR and 8R DIMM
- Up to maximum 2048 GB with 128 GB DRAM DIMM
- Follow updated JEDEC DDR4 specification with 288 pin DIMM socket
- Memory support matrix for DDR4 is as Table 3-1

2 Slots Per Channel	
1 DIMM Per Channel	2 DIMM per Channel
2666	2400

Table 5-2

5.3.3 AEP

Board and system design support Apache Pass DIMM with 128G, 256G and 512G.Max 12 AEP DIMMs with ADR function.

5.4 PCH

The motherboard uses Intel® Lewisburg chipset, which supports following features:

- 2x USB 3.0/2.0 ports: one x2 type A connector for front connector;
- 1x USB 2.0 for BMC in-band firmware update;
- 1x USB2.0 for X32 riser connector ;
- 1x M.2 connector on board(PCIe X4 Colay with SATA)；
- 1x individual SATA 6Gps port;
- 1x Oculink x4 connector use for SATA 0-3;
- 1x Oculink x4 connector use for PCIE 4X or SSATA 2-5;
- SPI interface, mux with BMC to enable BMC the capability to perform BIOS upgrade and Recovery
- SPI interface for TPM header
- SMBUS interface (master & slave)
- IntelR Server Platform Services (SPS) 4.0 Firmware with IntelR Node Manager
- PECI access to CPU
- SMLink0 connect to BMC
- IntelR Manageability Engine (ME) obtain HSC PMBus related information directly.
- IntelR ME SMLink1 connects to Hotswap controller PMBus interface by default.
- BMC has connection to HSC PMBus to have flexibility of HSC PMBus related feature support.
- Temperature sensors reading from BMC
- PCH SKUs
- Board design shall support all PCH SKUs in terms of power delivery and thermal design.

5.5 PCIe Usage

PCIe lanes are configured according to Table 5-3:

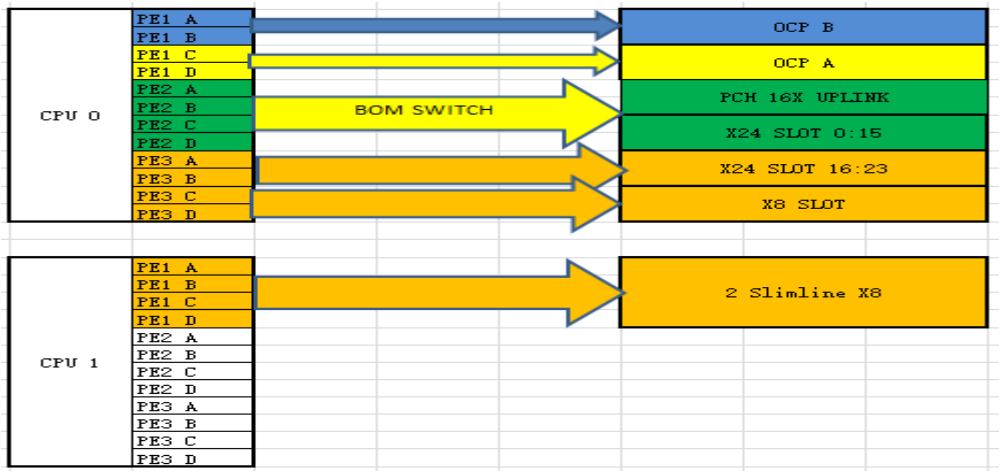


Table 5-3

5.6 PCB Stack Up

14 Layers Board Stack-Up For Purley_OCP_Rack
Overall Board Tickness: 97 +/-8%
Material : High TG， mid loss FR4 (S7038/IT170GRA1)

	Layer name	Plane Description	Material	Layer Thickness (mil) On pp	Layer Thickness (mil) On trace	Copper Weight(oz)	Dielectric Er	
	AIR							0.5
	solder mask	solder mask	Solder Mask	0.8	0.5	NA	3.8	1.9
L1	TOP	SIGNAL	Copper Plate / Copper Foil	1.9		0.5oz + Plating	NA	2.7 / 1.2
		prepreg	FR4	2.7		NA	4.0	3
L2	GND1/PWR	GND/PWR	Copper	1.2		1.0	NA	1.2
		CORE	FR4	3		NA	4.1	10
L3	Signal1	SIGNAL / GND	Copper	1.2		1.0	NA	1.2
		prepreg	FR4	10		NA	4.0	3
L4	Signal2	GND / SIGNAL	Copper	1.2		1.0	NA	1.2
		CORE	FR4	3.0		NA	4.1	4
L5	GND/PWR	GND/PWR	Copper	1.2		1.0	NA	1.2
		prepreg	FR4	4.0		NA	4.0	12
L6	Signal/PWR	PWR/UPI/Signal	Copper	1.2		1.0	NA	2.4
		CORE	FR4	12.0		NA	4.1	6
L7	PWR	PWR/GND	Copper	2.4		2.0	NA	2.4
		prepreg	FR4	6.0		NA	4.0	12
L8	PWR	GND/PWR	Copper	2.4		2	NA	1.2
		CORE	FR4	12.0		NA	4.0	4
L9	Signal/PWR	PWR/UPI/Signal	Copper	1.2		2.0	NA	1.2
		prepreg	FR4	4.0		NA	4.0	3
L10	GND/PWR	GND/PWR	Copper	1.2		1.0	NA	1.2
		CORE	FR4	3		NA	4.1	10
L11	Signal3	GND / SIGNAL	Copper	1.2		1.0	NA	1.2
		prepreg	FR4	10		NA	4.0	3
L12	Signal4	SIGNAL / GND	Copper	1.2		1.0	NA	1.2
		CORE	FR4	3		NA	4.1	2.7
L13	GND/PWR	GND/PWR	Copper	1.2		1.0	NA	1.9
		prepreg	FR4	2.7		NA	4.0	0.5
L14	BOTTOM	SIGNAL	Copper Foil / Copper Plate	1.9		0.5oz + Plating	NA	
	soldmask	solder mask	Solder Mask	0.8	0.5	NA	3.8	97
	AIR							2.463804928

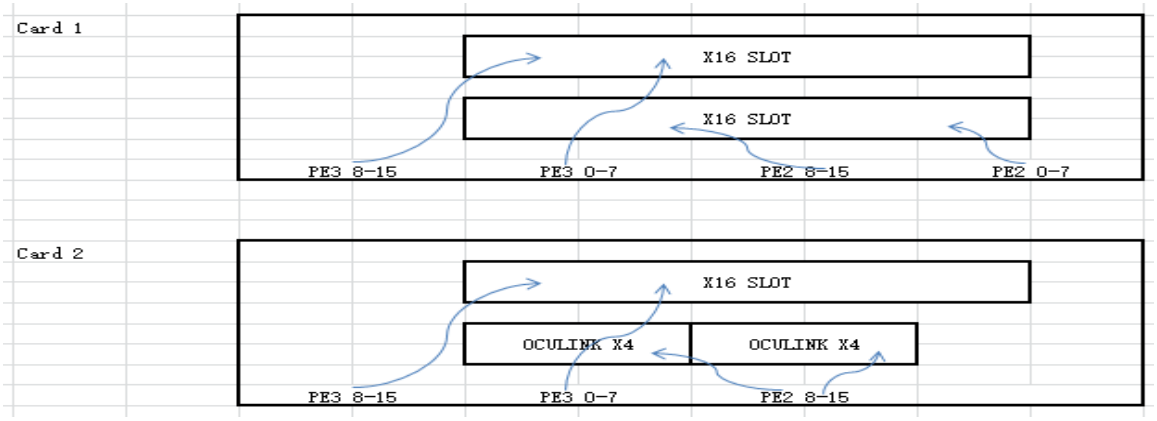
6 I/O System

This section describes the motherboard I/O system.

6.1 PCIe x32 Slot/Riser Card

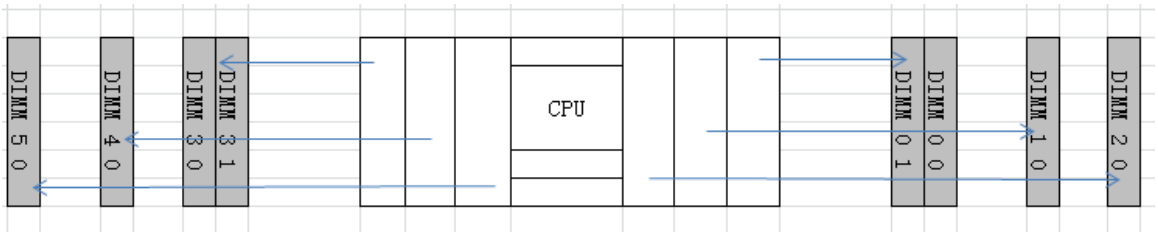
The motherboard has one 2x sockets to be used by PCIe riser cards. A x24 slot， All PCIe lanes to x32 PCIe is from CPU0. SMBus to BMC.

6.2 Riser Card Type



6.3 DIMM Slot

Total 16 DIMMs, DIMM 1 are Black, DIMM0 are White.



6.4 PCIe Mezzanine Card

The motherboard support OCP A/C Mezz cards. OCP A card has both Connector A and Connector B, support max PCIE 16X Mezz card.

Connector Pin definition follow the OCP Mezzanine Card 2.0 rev1.0.

6.5 Network

6.5.1 Data network

Use Single or Dual Port OCP MEZZ cards.

6.5.2 Management network

The motherboard has 3x options of management network interface for BMC's connection. Management network shares data network's physical interface. Management connection was independent from data traffic, and OS/driver condition.

a) 1 dedicated RJ45 port for Board management, driven by BMC through RMII/NC-SI.

b) 1 OCP A shared-NIC, driven by BMC through NCSI

c) 1 OCP C shared-NIC, driven by BMC through NCSI.

6.6 USB

The motherboard has one two ports external USB2.0/3.0 connector located in front of Motherboard. BIOS should support following devices on USB ports available on Motherboard:

- USB Keyboard and mouse
- USB flash drive (bootable)
- USB hard drive (bootable)
- USB optical drive (bootable)

6.7 SATA

The motherboard has Intel® Lewisburg PCH on board. Intel® Lewisburg has a SATA controller support 8x SATA3 ports, and an sSATA controller support 6x SATA3 ports.

- SATA Port 0~3 are connected to one vertical Oculink X4 connector.
- sSATA Port 2~5 are connected to another Oculink X4 connector. Can be configured to PCIe X4 for extra M.2 device
- sSATA Port 0 is connected to 1x M.2 connector on motherboard with dual layout with PCIe x4 to M2.
- sSATA Port 1 is connected to 1x vertical SATA connector on motherboard. Can be configured to extra SATA M.2 device

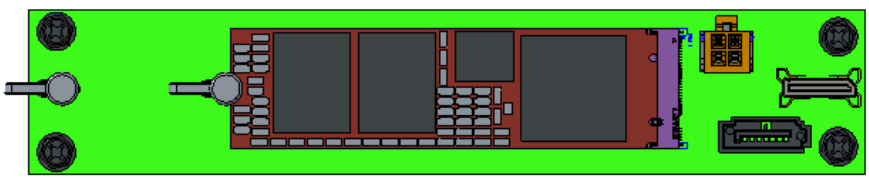
6.8 M.2

The motherboard supports two M.2 devices.

One is onboard co-layout between sSATA and PCIE X4.

The other one is on the M.2 carrier board. Optioned by cable to choose SATA or PCIE X4 interface.

Second M.2 on the carrier board：



6.9 Fan

Support total 3 FAN connectors in 1OU system or 2 FAN in 2OU system.

Pin 2: P12V max 3A.

Pin	Signal
1	GND
2	P12V
3	TACH0
4	PWM
5	TACH1
6	NC

6.10 LED

There are six LED on board:

► Power BTN LED, SW2

--After Press, Power on OK, Green; Power on Failure, RED.

► UID BTN LED: BLUE, SW3

-- BMC/SW3 Control it ON/OFF

► BMC FAULT LED: RED, LED2

--When BMC error occur, Turn ON.

► SPKR LED: YEL, LED4

--When system error occur, blinking.

► HDD ACT LED: Green, LED1

--When SATA/SSATA active, turn on.

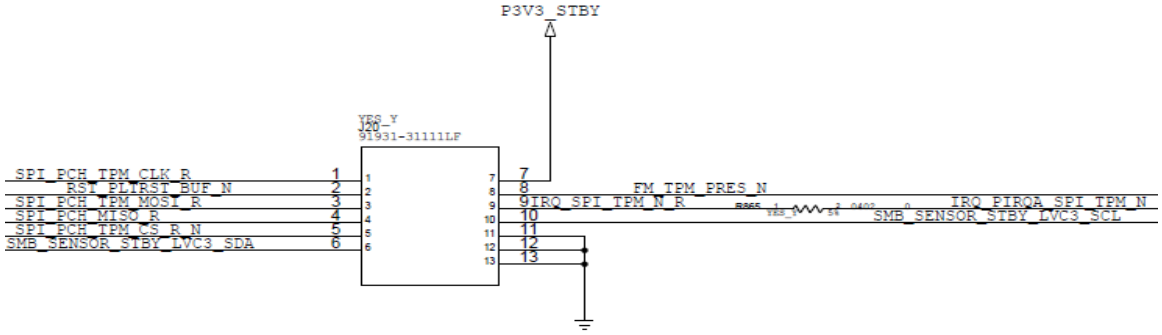
► BMC Heart Beat LED: Green, LED51

--When BMC active, Blinking.

6.11 TPM

Support one TPM connector with SPI and I2C interface.

SPI TPM controller for platform TPM and the I2C TPM controller for BMC secure boot.



6.12 Header

Features	Description (TYP,QTY)	Remark	接线缆/跳线帽
SATA RAID KEY	1x4	J41	
BMC I2C DEBUG&PCH SMLINK0 Header	1x3,BMC I2C5,PCH SML0	J32	
ME I2C DEBUG Header	1x3,HOST SMBUS	J33	
Clear CMOS Header	1x3,Pin2-3 means clear CMOS	J40	Default 1-2
I2C TO UART DETECT	1x3,Pin1-2 means no I2C to UART	J42	Default 2-3
ADR Delay Header	1x3,Pin2-3 means disable ADR DLY	J71	Default 2-3
BMC RST Header	1x3,Pin2-3 means rst BMC	J67	Default 1-2
CPLD UART CHANEL LOCKED Header	1x3,Pin2-3 means UART CHN fixed	J68	Default 1-2
ME Update Header	1x3, Pin2-3 means update ME	J21	Default 1-2
Clear BIOS PASSWORD Header	1x3, Pin2-3 means clear password	J29	Default 1-2
BIOS USB Recovery Header	1x3, Pin2-3 means USB recovery BIOS	J65	Default 1-2
BIOS TOP SWAP Header	1x3, Pin2-3 means BIOS TOP SWAP	J66	Default 1-2
OCP Trigger Point SET Header	1x3, Pin1-2: 48.8A;Pin 2-3:41.4A	J44	Default 1-2
MCP JTAG	2x5,x1	J9	
BMC/PCH/CPLD JTAG	2x5, x1	J63	
UV TRIGGER POINT SET	1X3, Pin 1-3	J43	Default 2-3

7 Reference Design and Difference

7.1 DIMM Slot can support Max 16 DIMMs in single side. Tiago Pass only support 12 DIMMs in single side.

7.2 With a UID Button for Node indicator; Tiago Pass only have one UID LED.

7.3 Design 3 fan connecters for cooling fan, support 2 * 8056 fan in 2OU, and 3 * 4056 fan in 1OU, at the same time obligate system fan control signal, the fans can work continue when the BMC die.

7.4 Support 2 * PCIE 3.0 x8 from CPU1 with slimline connecter.

7.5 With 2 * Oculink x4 connecter support SATA *8 or SATA *4 + 1 * PCIE x4 M.2.

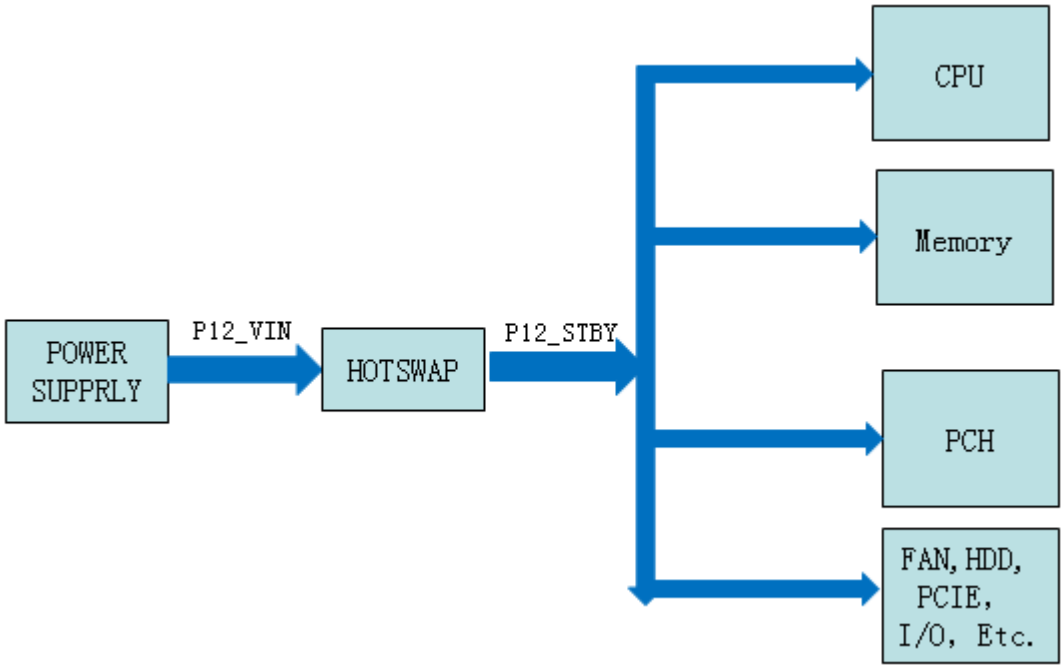
7.6 There is a power connecter with 8 pins support 1 * 3.5HDD / 2 * 2.5NVMe / PCIE 3.0 x16 carrier board / M.2 carrier board.

8 Motherboard Power system

8.1 Open Power budget

Power Rail	Vout(V)	CPU0 (A)	CPU1 (A)	MEM (A)	NVDIMM (A)	PCH (A)	BMC (A)	CLK (A)	Misc (A)	PCIE Slot 32X (A)	SATA HDD (A)	M.2 (A)	FAN (A)	OCP A (A	OCP B (A	OCP C (A)	USB3.0 (A
PVCCIN_CPU0	1.8	89															
PVSA_CPU0	0.85	15															
PVCCIO_CPU0	1	14															
PVCCMCP_CPU0	0.9	62															
P1V8_MCP_CPU0	1.8	8.5															
PVCCIOMCP_CPU0	1.03	20															
PVCCIN_CPU1			89														
PVSA_CPU1			15														
PVCCIO_CPU1			14														
PVCCMCP_CPU1			62														
P1V8_MCP_CPU1			8.5														
PVCCIOMCP_CPU1			20														
PVDDQ_ABC	1.2	16.9		48.96													
PVDDQ_DEF	1.2	16.9		48.96													
PVPP_ABC	2.5	0.3		6.6													
PVPP_DEF	2.5	0.3		6.6													
PVTT_ABC	0.6			1.71													
PVTT_DEF	0.6			1.71													
P12V_NVDIMM_ABC	12				1.4												
P12V_NVDIMM_DEF	12				1.4												
PVDDQ_GHJ		16.9		48.96													
PVDDQ_KLM		16.9		48.96													
PVPP_GHJ		0.3		6.6													
PVPP_KLM		0.3		6.6													
PVTT_GHJ				1.71													
PVTT_KLM				1.71													
P12V_NVDIMM_GHJ					1.4												
P12V_NVDIMM_KLM					1.4												
P12V_STBY														2.4	1.6	2.4	
P5V_STBY									0.5					2.4			2.7
P3V3_STBY						2	0.5		1.2	1				1.6			
PVNN_PCH_STBY						1.8											
P1V05_PCH_STBY						1.2											
P1V8_PCH_STBY						0.8											
P1V2_BMC_DDR4							0.5										
P1V15_AUX							1.3										
P3V3_AUX							0.4										
P12V										11	3		18				
P5V									1		2.5						
P3V3								0.7	0.8	6		3		6.4			

8.2 Power Simple Topology



8.3 Input voltage Level

The nominal input voltage delivered by the power supply is 12.5 VDC nominal at light loading with a range of 11V to 13V. The motherboard shall accept and operate normally with input voltage tolerance range between 10.8V and 13.2V when all under voltage related throttling features are disabled.

Motherboard's under-voltage protection level should be less than 10.1V.

8.4 Hot Swap Controller (HSC) Circuit

In order to have a better control of 12.5V DC power input to each motherboard, one HSC (ADI/ADM1278) is used on the motherboard. HSC circuit provides the following functions:

1. Inrush current control when motherboard is inserted and powered up.
2. Current limiting protection for over current and short circuit. Over current trip point should be able to set to 41.4A and 48.8A with jumper setting; default is 48.8A for SS. Over current trip point should be able to set to 71.5A and 78.9A with jumper setting; default is 71.5A for DS.
3. HSC UV protection shall be set to 10V~10.1V
4. SOA protection during MOSFET turning on and off.
5. HSC fault protection is set to latch off (default) with retry as stuff option.
6. PMBUS interface to enable PCH Intel ME and BMC following actions.
7. Use HSC or external circuit to provide fast (<20us) over current sense alert to trigger system

throttling and CPU fast PROCHOT#; feature need to be controlled by BMC GPIO directly. BIOS has a setting to control Enable/Disable/ [no change]. No change is the default. The means follow the BMC initial setting. BMC sets it to disable as the default, Before BMC is ready, and the hardware POR state is enable.

8. Use HSC or external circuit to provide fast (<20us) under-voltage alert to trigger system throttling and CPU fast PROCHOT#. This feature is enabled by default with resistor option to disable. The threshold is set to 11.5V by default and with option to set it 11V. The setting mechanism is from BMC.
9. Use HSC or external circuit to provide HSC timer alert to trigger system throttling before HSC OCP happens.
10. System, CPU, and memory Sub-system throttling set as Table 8-1.

Condition	Threshold	Action	Enable control	Default
Board input power over current limit	>40.6A or 47.9A[Default] by jumper setting for SS >70.8A[Default] or 76.8A for DS	Trigger throttle to system in < 20us	BMC GPIO	Disable
Board input power under voltage	<11.5V/11V	Trigger throttle to system in < 20us	Resistor option	Enable
Board input power under voltage	<11.5V/11V	Disable MOSFET between P12V_AUX to P12V_FAN	Resistor option	Disable
Board input power under voltage	<10.5V	Disable MOSFET between P12V_AUX to P12V_FAN	Resistor option	Enable
HSC Timer Alert	>400mV[10]	Trigger throttle to system in < 20us	Resistor option	Enable
CPU VR hot	Determined by CPU VR design	Trigger throttle to PROCHOT in < 20us	N/A	Enable (always)
Memory VR hot	Determined by Memory VR design	Trigger throttle to MEM_HOT in < 20us	N/A	Enable (always)

Table 8-1 Entry point of System, CPU, and memory Sub-system throttling

11. The voltage drop on HSC current sense resistor should be less or equal to 25mV at full loading. Hot swap controllers should have SMBUS address set to 0x11 (7bit format) on single side with 0.5mohm Rsen, 0x45 (7bit format) on double side with 0.25mohm Rsen.
12. The power reporting of hot swap controller needs to be better than +/-2% from 50W to full loading in room temperature as a minimal requirement. Vendor shall optimize HSC power reporting by taking measurement on multiple samples and using firmware to apply different offset based on system loading and temperature.

8.5 CPU & Memory VR

CPU VR follow latest VR13 SPEC，it shall be designed to handle a processor with a maximum TDP of 165W, for Intel Skylake-SP. Support for processors of higher TDP is not required. As a result the vendor shall optimize the CPU VR accordingly.

8.5.1 DIMM VR

Using the minimum number of total phases to support the maximum CPU power. CPU VR have auto phase dropping feature, and run at optimized phase count among 1, 2, 3,…, and maximum phase count. CPU VR support all Power States to allow the VRM to operate at its peak efficiency at light loading

8.5.2 DIMM VR

DIMM VR support auto phase dropping for high efficiency across loading. DIMM VR compliant to latest VR13 specification.

8.5.3 Detail design

Power Rail	VOUT	VIN	VR Type	VR QTY/ BRD	VR Controller IC and FET	Smbus Address
PVCCIN_CPU0 PVCCIN_CPU1	sVID	P12V_STBY	Switcher	2	Infineon PXM1610C+6Phase TDA21470;5Phase for PVCCIN_CPU;1Phase for PVCCSA	CPU0:0X90 CPU1:0XB0
PVCCSA_CPU0 PVCCSA_CPU1	sVID	P12V_STBY	Switcher	2		
PVCCIO_CPU0 PVCCIO_CPU1	sVID	P12V_STBY	Switcher	2	Infineon PXE110C+1PhaseTDA21470	PVCCIO_CPU0:94 PVCCIO_CPU1:B4
PVMCP_CPU(VRM)	sVID	P12V_STBY	Switcher	1	Infineon PXM1310C+3Phase TDA21470	PVMCP_CPU0:98 PVMCP_CPU1:B8
P1V8_MCP_CPU(VRM)	1.8V	P12V_STBY	Switcher	1	Infineon PXE110C+2 PhaseTDA21470;1Phase for P1V8_MCP,1Phase for PVCCIOMCP	PXX_MCP_CPU0:C4 PXX_MCP_CPU0:C8
PVCCIOMCP_CPU(VRM)	sVID	P12V_STBY				

PVDDQ_ABC PVDDQ_DEF PVDDQ_GHJ PVDDQ_KLM	1.2V	P12V_STBY	Switcher	4	Infineon PXM1310C+2Phase TDA21470	PVDDQ_ABC:0X50 PVDDQ_DEF:0X54 PVDDQ_GHJ:0X70 PVDDQ_KLM:0X74
PVTT_DDR_ABC PVTT_DDR_DEF PVTT_DDR_GHJ PVTT_DDR_KLM	1/2*PVDDQ_xx	PVTT_DDR_ABC PVTT_DDR_DEF PVTT_DDR_GHJ PVTT_DDR_KLM	LDO	4	TPS51200DRCR	
PVPP_DDR_ABC PVPP_DDR_DEF PVPP_DDR_GHJ PVPP_DDR_KLM	2.5V	P12V_STBY	POL	4	TPS53319DQPR	
P12V_STBY	12.5V	P12V_IN	HOT SWAP	1	ADM1278	
P5V_STBY	5V	P12V_STBY	POL	1	TPS53319DQPR	
P3V3_STBY	3.3V	P12V_STBY	POL	1	TPS53319DQPR	
PVNN_PCH_STBY	0.85V, 0.9V, 0.95V or 1.0V	P12V_STBY	Switcher	1	PXE1110C+2Phase TDA21470; 1Phase for PVNN_PCH_STBY,1Phase for P1V05_PCH_STBY	0XD0
P1V05_PCH_STBY	1.05V	P12V_STBY				
P1V8_PCH_STBY	1.8V	P3V3_STBY	LDO	1	TPS7A7200RGTT	

Power Rail	VOUT	VIN	VR Type	VR QTY/BRD	VR Controller IC and FET	Smbus Address
P1V2_BMC_DDR4	1.2V	P3V3_STBY	LDO	1	TPS7A7200RGTT	
P1V15_AUX	1.15V	P3V3_STBY	LDO	1	TPS7A7200RGTT	
P2V5_AUX	2.5V	P3V3_STBY	LDO	1	TPS7A7200RGTT	
P12V	12.5V	P12V_STBY	E-fuse	1	VT505	
P5V	5V	P12V_STBY	E-fuse	1	TPS22959DNYR	

P3V3	3V3	P3V3_STBY	POL		TPS53353DQPR	

9 BIOS

9.1 BIOS Description

9.1.1 BIOS Chip

The BIOS chip use PCH's SPI interface through BMC controlled MUX.

Item	Description
Code Base Vendor	AMI AptioV
BIOS Image Size	16MB
ROM Image Size	32MB

9.1.2 BIOS Source Code

BIOS Code based on AMI Purley NeonCity CRB code, using Intel EDKII software architecture.

9.2 BIOS Features

9.2.1 BIOS Supported Specifications

- Multiprocessor Specification, Version 1.4.
- PCI BIOS Specification, Version 2.1.
- PCI-to-PCI Bridge Architecture Specification, Version 1.2.
- PCI-X Addendum to the PCI Local Bus Specification Version 1.0A
- BIOS Boot Specification (BBS), Version 1.01.
- PCI Express Base Specification Version 1.0a
- PCI Express Base Specification Version 2.0
- PCI Express Base Specification Version 3.0
- PCI Local Bus Specification Version 3.0
- PCI Firmware Specification Version 3.1
- Advanced Configuration and Power Interface Specification 5.0
- System Management BIOS (SMBIOS) Specification 2.7.1 or later
- Plug and Play BIOS Specification, Revision 1.0a

- PC System Design Guide 2001 - Any conflict occurs between Windows Logo Program System and Device Requirements and, follows Windows Logo Program System and Device Requirements.
- Serial ATA Specification 3.0
- AHCI Specification 1.3
- EDD (BIOS Enhanced Disk Drive) Specification V3.0 Revision 0.8
- "El Torito" Bootable CD-ROM Format Specification, Version 1.0
- Final version (approved by PC Client Workgroup) of TCG
- Functionality and Interface Specification of Cryptographic Support Platform for Trusted Computing (Chinese TCM)
- UEFI Specification 2.3.1 or later
- UEFI PI Specification 1.2 or later
- UEFI SCT 2.3
- NIST 800-147 BIOS Protection Guidelines
- NIST 800-147B BIOS Protection Guidelines for Server
- Intelligent Platform Management Interface Specification V2.0

9.2.2 BIOS Error Handle

- BIOS support IPMI SEL Log
- BIOS support PCIe IOAPIC、x2apic
- BIOS support machine check error
- BIOS support DDR4 command/Address parity check
- BIOS support memory mirroring
- BIOS support memory demand/patrol scrubbing
- BIOS support HA/IMC corrupt Data Containment
- BIOS support memory rank/multi rank sparing
- BIOS support address based memory mirroring
- BIOS support QPI dynamic link width reduction
- BIOS support Intel QPI Clock Fail over
- BIOS support PCI Express Advanced Error Reporting
- BIOS support PCI Express Enhanced Root Port Error Reporting
- BIOS support EMCA gen 2

9.2.3 BIOS Setup Screen

- BIOS setup options are including but not limited to the following options
- BIOS setup support modify core number
- BIOS setup support enable/disable HT
- BIOS setup support enable/disable VT-X/VT-D/SR-IOV
- BIOS setup support enable/disable prefetch
- BIOS setup support display CPU L1/L2/L3
- BIOS setup support enable/disable turbo boost
- BIOS setup support enable/disable p-state
- BIOS setup support enable/disable c-state
- BIOS setup support enable/disable PCIe ASPM
- BIOS setup support enable/disable patrol scrubbing
- BIOS setup support enable/disable memory scrambling
- BIOS setup support enable/disable PXE boot
- BIOS setup support performance/efficient/custom

- BIOS setup support EIST
- Setup Layout Reference：Purley Platform BIOS layout0.5（AMI）

9.2.4 SMBIOS

Type	function
0	BIOS Information
1	System Information
7	Cache Information
8	Port Connector Information
9	System Slots
11	OEM Strings
12	System Configuration Options
13	BIOS Language Information
16	Physical Memory Array
20	Memory Device Mapped Address
32	System Boot Information
38	IPMI Device Information
39	System Power Supply
41	Onboard Devices Extended Information
127	End of Table

9.2.5 Boot

- BIOS Support SAS、SATA, AHCI and PXE boot.
- BIOS Support Change boot priority
- BIOS support UEFI Network Stack
- BIOS support IPMI modify BOOT sequence
- BIOS support Boot Retry :

Enable: If there is no bootable device found, BIOS should keep loop searching for bootable device.

Disable: If there is no bootable device found, BIOS will stop boot and show ”Reboot and Select proper

Boot device or Insert Boot Media in selected Boot device and press a key". BIOS should support UEFI and legacy boot mode options, UEFI and legacy boot mode have independent boot loop.

9.2.6 BIOS Update

- BIOS support USB Storage Device Recovery
- BIOS support Update BIOS Image through BMC
- BIOS support Update BIOS in UEFI Shell、Windows OS & Linux OS
- BIOS support remote refresh

10 BMC

10.1 BMC Description

10.1.1 BMC Chip

The BMC chip use Aspeed AST2500.

Item	Description
Code Base Vendor	AMI
BIOS Image Size	32MB
ROM Image Size	64MB

10.1.2 BMC Source Code

BMC Code based on AMI BMC source code, using AMI BMC software architecture.

10.2 BMC Features

10.2.1 BMC Supported Specifications

10.2.1.1 IPMI 2.0

- IPMI 2.0 for Standard IPMI Spec.
- IPMI 2.0 for Asset Information.
- IPMI 2.0 for Status Monitor.
- IPMI 2.0 for BIOS Post SEL Log.
- IPMI 2.0 for Network Switch & Control
- IPMI 2.0 for BIOS Option Monitor & Configure
- IPMI 2.0 for Other OEM Command

10.2.1.2 Web-based GUI

- Server Power Control
- Locate Server
- BMC Network Setting
- Service Setting
- NTP Setting
- BMC Self Inspection Result
- BMC Recovery
- Host Post Code
- Restory Factory Defautls
- Web Summary
- Asset Information
- Console Redirection
- Virtual Media
- Mouse Mode
- Fan Speed Control (Manual)
- ShareNic Switch
- BMC System Audit log
- Event Log Setting
- System Audit Log Setting
- User Administrator
- Dual Image Configure
- Dual Firmware Update
- BIOS FW Update
- System Event log with Severity
- System Event log Export
- BMC System Audit log Export
- Screen Capture
- Operator Log (Audit Log)
- Syslog Log
- Boot Order Setting

10.2.1.3 Connectivity

- Share NIC
- Dedicated NIC
- VLAN tagging
- IPV4
- DHCP
- IPV6

10.2.1.4 Security

- Role-based authority
- Local users

- SSL encryption

10.2.1.5 Remote Presence

- Serial-over-LAN
- Virtual Media
- Virtual Console
- Power control

10.2.1.6 Power & Thermal

- Temperature monitoring
- Thermal control

10.2.1.7 Diagnostics, Service, & Logging

- Health LED

10.2.1.8 Update

- BMC support Web-based Update.
- BMC support update under UEFI shell, windows OS, Linux OS

11 Thermal Design Requirements

To meet thermal reliability requirement, the thermal and cooling solution should dissipate heat from the components when system operating at its maximum thermal power. The thermal solution should be found by setting a high power target for initial design in order to avoid redesign of cooling solution; however, the final thermal solution of the system should be most optimized and energy efficient under data center environmental conditions with the lowest capital and operating costs. Thermal solution should not allow any overheating issue for any components in system.

11.1 Data Center Environmental Conditions

The thermal design for Intel Motherboard V4.0 needs to satisfy the data center operational conditions as described below.

11.1.1 Altitude

Data centers could be located up to 2500 meters above sea level.

11.1.2 Cold-Aisle temperature

Data centers will generally maintain cold aisle temperatures between 18°C and 30°C (65°F to 85°F). The mean temperature in the cold aisle is 24°C with 3°C standard deviation. The

cold aisle temperature in a data center may fluctuate minutely depending to the outside air temperature of data center. Every component in system must be cooled and maintained below its maximum spec temperature in any of cold aisle temperature in a data center.

11.1.3 R.H

Most data centers will maintain the relative humidity to be between 20% and 85%. In the thermal design, the environmental condition changes due to the high altitude may not be considered when the thermal design can meet the requirement with maximum relative humidity, 85%.

11.2 Server operational condition

11.2.1 Inlet Temperature

The inlet air temperature will vary. The cooling system should cover inlet temperatures as 20C, 25C, 30C, and 35C. Cooling above 30C is beyond operating specification, but used during validation to demonstrate design margin. CPU throttling is not allowed to activate over the validation range 0C – 35C.

11.2.2 Fan Redundancy

The server fans at N+1 redundancy should be sufficient for cooling server components to temperatures below their maximum spec to prevent server shut down or to prevent either CPU or memory throttling.

11.2.3 Thermal Margin

The thermal margin is the difference between the maximum theoretical safe temperature and the actual temperature. The board design operates at an inlet temperature of 35°C (95°F) outside of the system with a minimum 2% thermal margin for every component on the card. Otherwise, the thermal margin for every component in the system is at least 7% for temperatures up to 30°C.

11.3 Thermal kit requirements

11.3.1 Heat Sink

The heat sink design should choose to be most optimized design with lowest cost. The heat sink design should be reliable and the most energy efficient design that satisfies all the

conditions described above.

11.3.2 System Fan

The system fan must be highly power-efficient with dual bearing. The propagation of vibration cause by fan rotation should be minimized and limited. The frame size of fan is 80x80x56mm.

11.3.3 Air-Duct

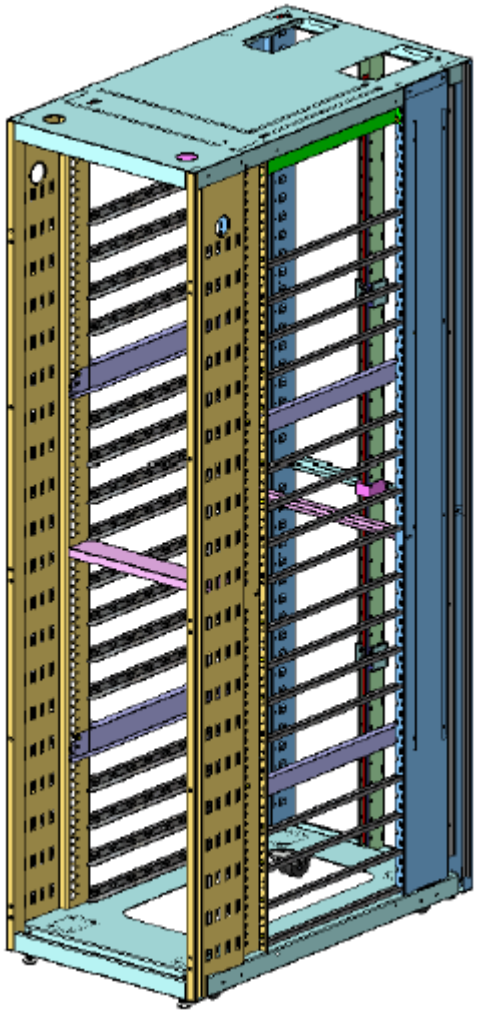
The air duct needs to be part of the motherboard tray cover, and must be most energy efficient design. The air-duct design should be simple and easily serviceable. The air-duct design should be unified for all SKUs. Using highly green material or reusable material for the air duct is preferred.

11.3.4 Thermal sensor

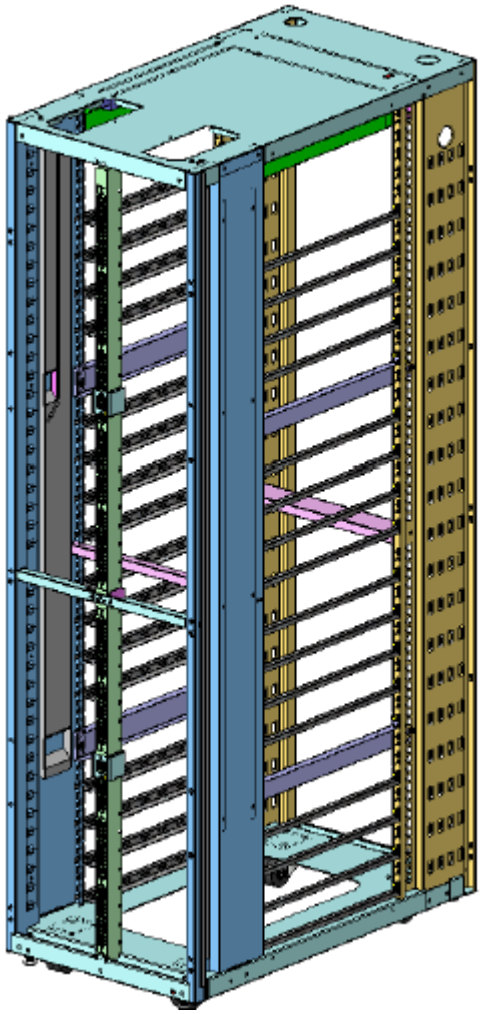
The maximum allowable tolerance of thermal sensors in the motherboard is ±3°C.

12 ORv2 Implementation

12.1 Rack for ORv2

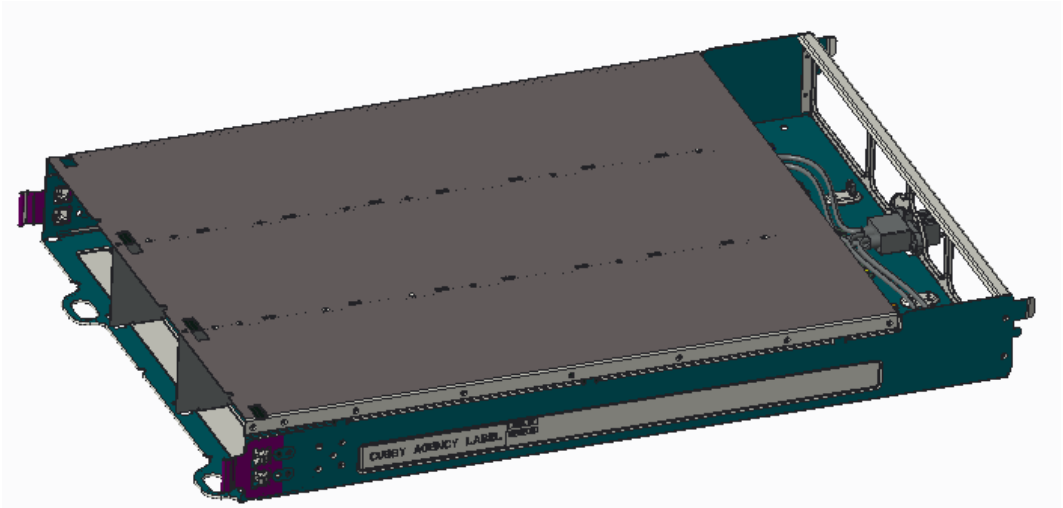


12.2 Bus Bar for ORv2

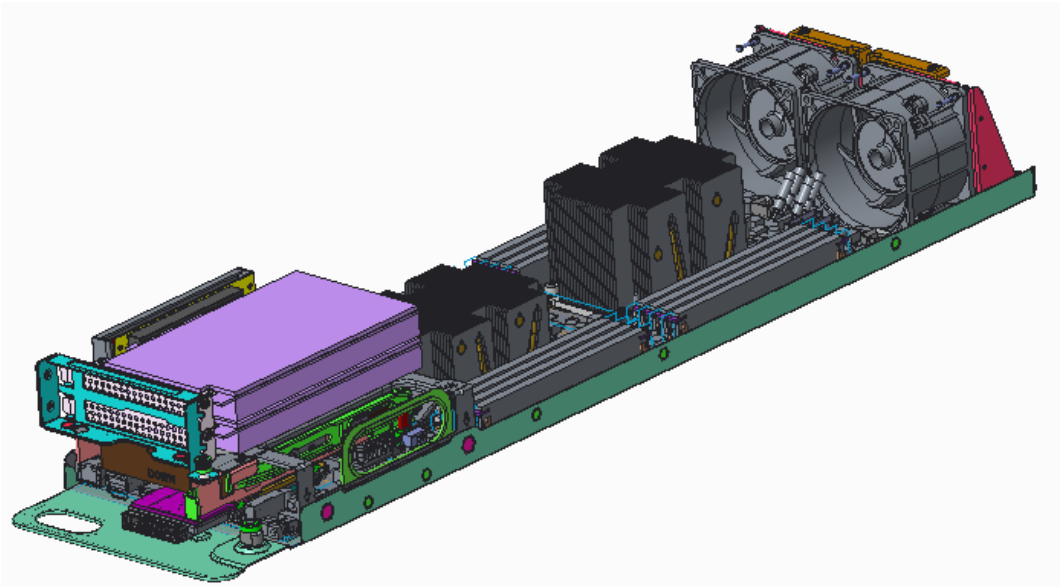


12.3 Cubby for ORv2

Cubby enclosure for Intel Motherboard V4.0 - ORv2 sled. Cubby serves as the mechanical and power delivery interface between ORv2 and Intel Motherboard V4.0-ORv2 sled.

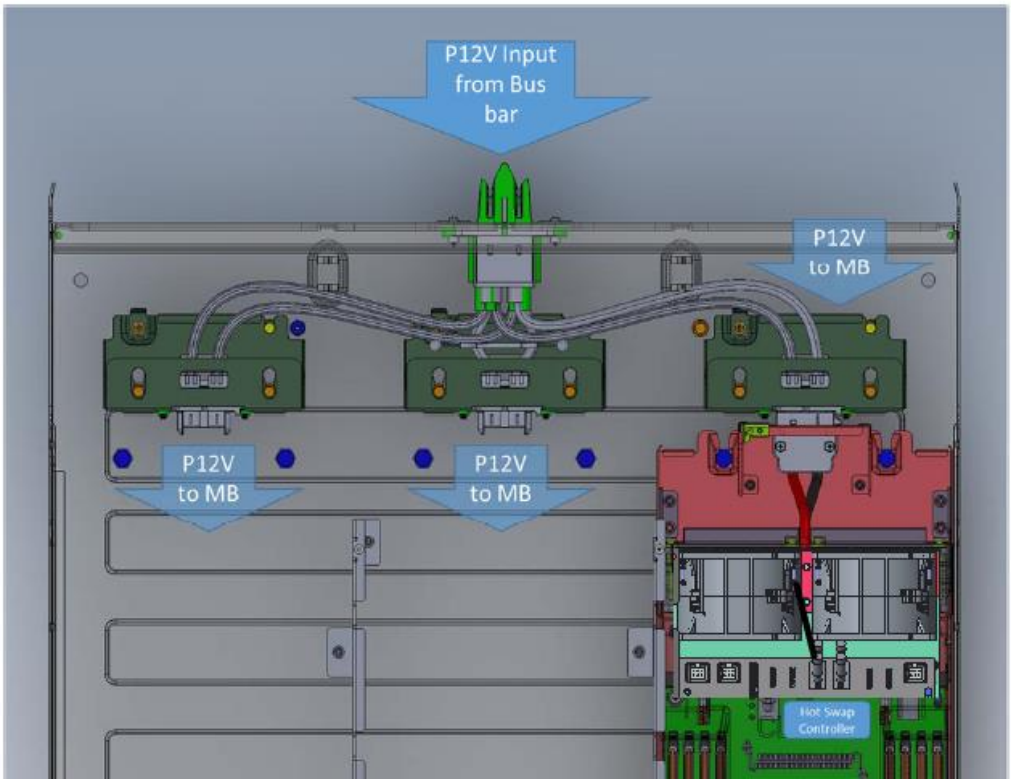


12.4 Bay for ORv2



12.5 Intel Motherboard V4.0-ORv2 Power Delivery

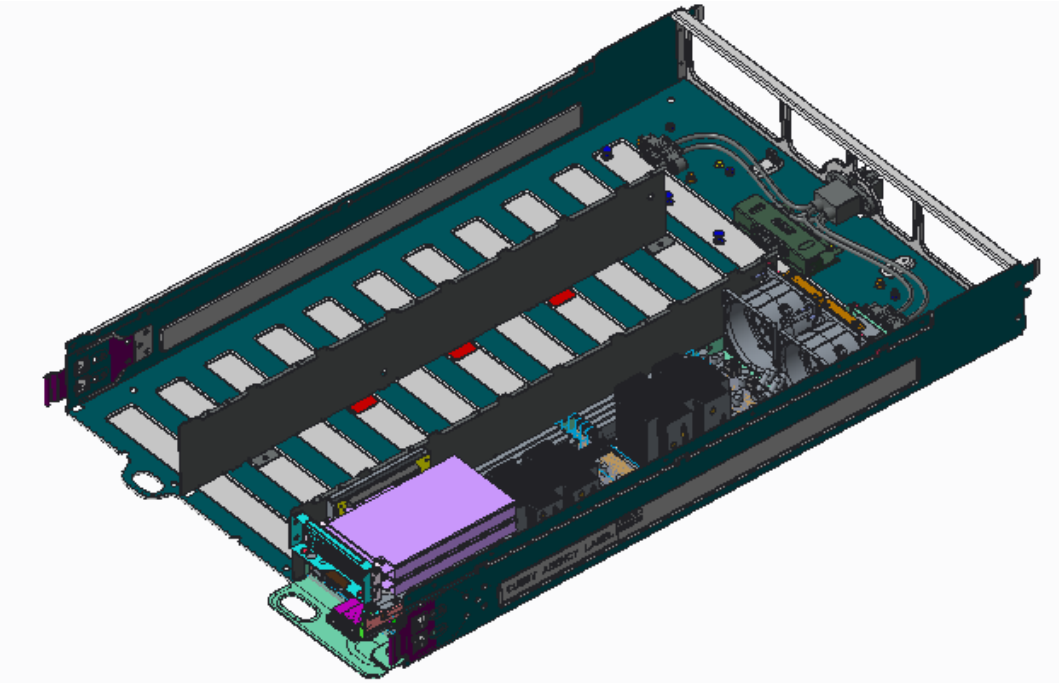
There is one bus bar in each power zone of ORv2. There are up to 3x sleds in each cubby enclosure.



12.6 Intel Motherboard V4.0-ORv2 single side sled

Single side Sled supports up to 16x DIMM slots. All DIMM slots are on the component side of

motherboard.



13 Mechanical

13.1 Fixed Locations

Refer to mechanical DXF file for fixed locations of mounting hole, PCIe x16 slot and power connector.

13.2 PCB Thickness

To ensure proper alignment of the motherboard and mid-plane interface within its mechanical enclosure, the motherboard PCB thickness is 97mil (2.46mm). And mid-plane PCB thickness should also be 89.4mil (2.27mm). Mezzanine card and riser card PCB thickness should be 62mil (≈1.57mm).

13.3 Heat Sinks and ILM

The motherboard shall support heat sinks that are mounted according to the Intel's E5-2600 v3 thermal mechanical specification and design guide. The vendor shall comply with all keep out zones defined by Intel in the above referenced specification. Standard LGA2011-3 heat sink and Narrow ILM solution is preferred. Only when vendor's CPU/VR placement doesn't allow standard Intel heat sink and Narrow ILM to be used, the vendor may choose non-standard heat sink, however this may require approval from the entity purchasing the motherboard.

13.4 Silk Screen

The color of silk screen is white and the labels for the components are listed as below.

- CPU0 / CPU1
- DIMM slot numbering should be described as blow:

	code
C P U 0 (Channel 0 & 1)	A0
	A1
	A2
	A3
C P U 0 (Channel 2 & 3)	A4
	A5
	A6
	A7
C P U 1 (Channel 0 & 1)	B0
	B1
	B2
	B3
C P U 1 (Channel 2 & 3)	B4
	B5
	B6
	B7

- LEDs are defined as blow:

LED Color	Fuction	Silk Screen Label
Blue	Power LED. This LED shall illuminate if the motherboard is in the power on state. This LED is also used as chassis identify.	PWR
Green	Hard drive activity. This LED shall illuminate when there is activity on the motherboards SATA hard drive interfaces, or onboard mSATA and M.2 connector interface.	HDD
Yellow	BEEP/Error LED. This LED shall illuminate when PCH speaker has output , or , BIOS_ERR_TRIGGER_N asserts. BIOS_ERR_TRIGGER_N is for debug purpose to have a predefined error identified from LED. It can also be used as oscilloscope trigger. It is disabled in production BIOS.	BEEP/ERR
Green	UART Channel status LEDs. Two LEDs indicates the UART channel number's binary code. Both LEDs should stay off by default to indicate UART channel is on host console. Smaller package should be used for these two LEDs compare to the other three.	UART_CH(1..0)

- Switches as PWR and RST

Vendor need to provide CB reports of the motherboard and tray in component level. These documents are needed to have rack level CE. The sled should be compliant with RoHS and WEEE. The motherboard PCB should have UL 94V-0 certificate. The vendor should design an EMI panel kit and pass FCC Class A.

13.5 DIMM Connector Color

Colored DIMM connectors shall be used to indicate the first DIMM of each memory channel. This first DIMM on each channel is defined as the DIMM placed physically furthest from its associated CPU. This DIMM connector shall be populated first when the memory is only partially populated. The First DIMM connector shall be a different color than the remaining DIMM connectors on the same memory channel.

13.6 PCB Color

The color of PCB include every revision is Green.

14 Labels and Markings

14.1 Labels

The motherboard shall include the labels such as adhesive and silk screen labels on the component side of the motherboard.

14.2 Markings

The motherboard shall include the markings such as adhesive and silk screen markings in accordance with required international certification.

15 Prescribed Materials

15.1 Disallowed Components

The following components shall not be used in the design of the motherboard.

- Components disallowed by the European Union`s Restriction of Hazardous Substances Directive (RoHS)
- Trimmers and/or Potentiometers
- Dip Switches

15.2 Capacitors & Inductors

The following limitations shall be applied to the use of capacitors

- Only Aluminum Organic Polymer Capacitors shall all be used they must be rated 105C, and shall be selected only from Japanese Manufacturers.
- All capacitors will have a predicted life of at least 50,000 hours at 45C inlet air temperature,

under worst conditions.

- Do not use Tantalum capacitor
- SMT Ceramic Capacitors with case size > 1206 are not preferred. Vendor shall discuss with Facebook before using MLCC > 1206 case by case. Size 1206 still allowed when installed far from PCB edge, and with a correct orientation that minimizes risks of cracks.
- X7R Ceramics material shall be used for SMT capacitors by default. COG or NP0 type should be used in critical portions of the design. X6S can be used in CPU Cage area. Vendor shall discuss with Facebook before using X5R with evaluation of worst case temperature of the location.
- Only SMT inductors may be used. The use of through-hole inductors is disallowed.

15.3 Component De-rating

For inductors, capacitors and FETs, de-rating analysis should be based on at least 20% derating.

16 Reliability and Quality

16.1 Temperature and Humidity

The motherboard can run between 0℃ and 40℃ for long periods。And the motherboard can run in the relative humidity between 10% and 90% for long periods. The motherboard can run in a bigger temperature range for a short time， in the HALT(Highly accelerated life test),the motherboard can run at -30℃ and also can run at 70℃。

16.2 Specification Compliance

Inspur ensures that the motherboard meets these specifications as a stand-alone unit and while functioning in a complete server system. Inspur is ultimately responsible for assuring that the production motherboards conform to this Specification with no deviations. Inspur exceed the quality standards demonstrated during the pilot build (PVT) while the motherboard is in mass production。Customer must be notified if any changes are made which may impact product quality.

16.3 Change Orders

Inspur will notify customer any time a change is made to the motherboard. A Specification Compliance Matrix will be submitted to customer for each revision of the motherboard including

prototype samples.

16.4 Failure Analysis

Inspur will perform failure analysis on defective units, which are returned to the Inspur. Feedback shall be provided to customer with a Corrective Action plan within two weeks from the date, which the units were received at Inspur's Facility.

16.5 Warranty

Inspur warrants the motherboard against defects and workmanship for a period of two years from the date of initial deployment at customer's facility. The warranty is fully transferable to any end user.

16.6 MTBF Requirements

The motherboard has a minimum calculated MTBF of 170K hours at 90% confidence level at 45C ambient temperature. The motherboard also demonstrates the MTBF requirement above by running at full load and 50% of time and performing AC cycling test 50% of time at 45C. Typical alternation period is 1 week for stress test and 1 week for AC cycling test. This MTBF demonstration shall finish prior to First Customer Shipment (Pilots samples, Mass Production units). The motherboard shall have a minimum Service Life of 5 years (24 Hours / day, Full Load at 45C ambient temperature).

16.7 Quality Control

Below is a list of Inspur's product quality:

- Incoming product has less than 0.1% rejections
- Cpk values exceeds 1.33 (Pilot Build & Production)
- Inpsur will implement a quality control procedure during Production, by sampling motherboards at random from the production line and running full test to prove ongoing compliance to the requirements. This process shall be documented and submitted prior to Production. The relative reports shall be submitted on an ongoing basis.
- Inpsur will conduct an ongoing burn-In procedure for use in Production (Production will not start without an agreement on some sort of burn-in procedure). Vendors shall submit documentation detailing the burn in procedure

16.8 Change Authorization and Revision Control

After the motherboard is released to mass production, no design changes, AVL changes,

manufacturing process or materials changes are allowed without prior written authorization from customer. The AVL (Approved Vendor List) is defined by the list of components specified in the BOM (Bill of Materials). Any request for changes must be submitted to customer with proper documentation showing details of the changes, and reason for the changes. This includes changes affecting form, fit, function, safety, or serviceability of the product. Major changes in the product (or in the manufacturing process) will require re-qualification and/or recertification to the Product. A new set of First Article Samples may be required to complete the ECO process. Any modifications after approval shall phase-in during production without causing any delays or shift of the current production schedule. Vendors shall provide enough advance notice to customer to prevent any discontinuation of production. All changes beginning with the pilot run must go through a formal ECO process. The revision number (on the motherboard label) will increment accordingly. Revision Control: copies of all ECOs affecting the product will be provided to customer for approval.

16.9 PCB Tests

Inpsur will arrange Independent 3rd party lab testing on Delta-L, IST, and IPC-6012C for each motherboard, riser card and mid-plane PCB from every PCB vendors. Midplane without high speed differential signal does not require SET2DIL test. Inpsur do not use the PCB vendor for these tests. Inpsur will submit reports for review and approval before a PCB vendor can be used in mass production. The testing lots will be manufactured at the same facility of a PCB vendor with same process that planned to be used by mass production. Delta-L requires 5x different PCB fabrication lots from the PCB vendor, 30pcs coupons each time. Environmental shipping, packaging, and handling of this board is vital to test success; overnight shipping direct from PCB vendor to Delta-L independent lab is recommended. IST is done once. It is to IST test during DVT stage. It is required to be tested on a board manufactured at the same time as a board that completely passes Delta-L. (Run Delta-L, if it passes then ask the IST lab to run IST on the board they receive.) IST test profile is 3x cycles to 250°C and up to 1000x cycle to 150°C. Passing criteria is 150x cycles average, and 100x cycles minimum for 35x coupons.IPC-6012C is done when 2x of the 5x Delta-L tests passing from a PCB vendor. (Passing at the independent test lab) Inpsur will also request each PCB vendor to provide 30pcs Impedance coupon measurements and X-section check reports for each stage. Inpsur will work with PCB house to implement

Impedance, IST and Delta-L coupon to break off panel without increasing unit cost of PCB. These coupons will be on a working panel for riser cards or mid-plane board.

16.10 Secondary Component

Secondary component planning will start from DVT and reach 70% of total number of BOM items in PCBA BOM in DVT. PCB is planned with 2 vendors at EVT. EVT and DVT build plan will cover all possible combinations of key components of DC to DC VR including output inductor, MOSFETs and driver.

17 Deliverables

17.1 OS Support

Motherboard shall support CentOS 7.3 64-bit with updated Kernel specified customer, and pass Red Hat certification tests.

17.2 Accessories

All motherboard related accessories, including heat sink, button battery and CPU socket protectors, should be provided and installed at the vendor's factory. All accessory boards including debug card, PCIe riser card, should be provided by the vendor.

17.3 Documentation

The vendor shall supply the following documentation to customer:

- Full CAD-generated system schematic
- System board layout including timing constraints and stack up (CAD)
- BOM
- PCB files in RS-274x or other open format
- Schematic board component placement map
- 3D CAD generated drawing of the top level assembly, housing and all parts and subparts in CAD-neutral format such as STEP or IGES
- All FW, Tools and drivers in binary form that are required to boot and operate the product within the definition of the spec and are compatible with at least one major freely available OS (Linux) or commercial (Windows)

17.4 Mass Production First Article Samples

Prior to final project release and mass production, the Vendor will submit the following samples and documentation:

- All the pertinent documentation described in section 17.3 and any other documents and reports, necessary for customer to release the product to mass Production.
- User Manual.
- A full Test/Validation Report.
- Production line final Test ‘PASS’ tickets.
- Samples shipped using the approved for production-shipping box.

18 Shipping

The motherboard shall be shipped using a custom packaging containing multiple motherboards in each package. The quality of the packing assembly will be such that the motherboard will not get damaged during transportation. The units shall arrive in optimum condition and will be suitable for immediate use. Shock Test for the shipping box shall be conducted by the Vendor and submitted to customer for audit and approval.