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Compute Project

Inspur Mission Bay 3OU 8 GPU JBOG System Specification V0.1

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Page 1 of 1

2: Scope

This document defines the technical specifications for the Open Compute Project Mission Bay 8 GPU

3: Overview

The Mission Bay will be contents 8 GPU base board that supports NVIDIA SXM2 GPU to provide a flexible feature set between technology leadership and cost.

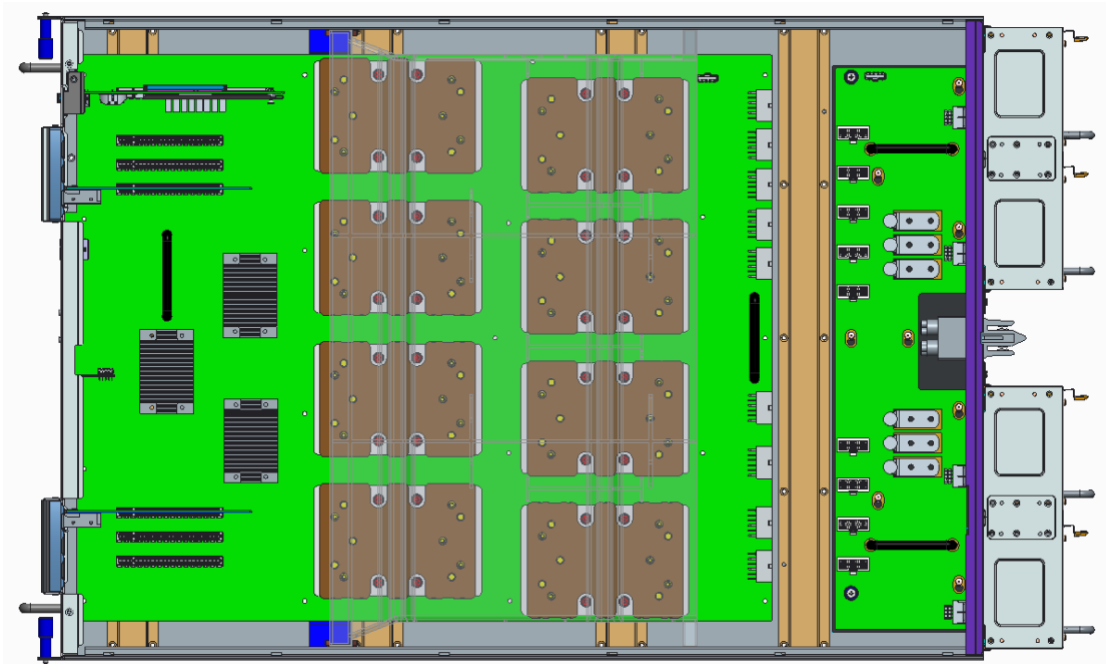


Figure 1: system top view



Figure 2: system front view

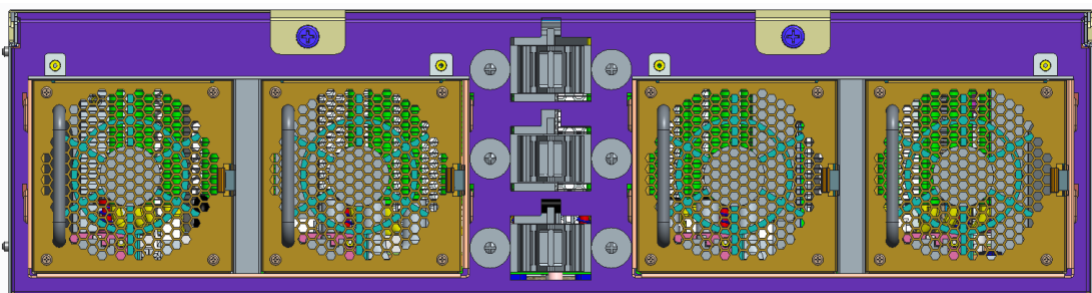


Figure 3: System rear view

4: Feature Requirements

4.1: PCB/Switch/GPU

Features		Description	Remark
PCB	Form Factor	No Standard	Inspur
	Layer	16	
	Color	Green	
	Board Size	450X590MM	
Switch	Type	PLX9797	
	Vendor	Broadcom	
	PCIE	PCIE 3.0	
	Lane	97 lanes	
	Thermal shutdown	Yes	
GPU	Type	SXM2 V100、P100	
	Vendor	INVIDIA	
	Port	2个PCIe3.0 x8 P100: 4个NVLink1.0 x8 V100: 6个NVLink2.0 x8	
	Thermal shutdown	Yes	

4.2 :Memory/Clock/Storage

Features	Description	Remark
Memory	No	
Generator	5P49V5901A750NLGI8	
Clock Buffer	9ZX21901BKLFT 9DB834AGILFT	

4.3: PCIE Slot

Features	Description	Remark
PCIEX16	PCIE A0, PEXA<16:31>, UP Stream	J40
PCIEX16	PCIE A1, PEXA<80:95>, Down Stream	J29
PCIEX16	PCIE A2, PEXC<80:95>, Down Stream	J30
PCIEX16	PCIE B0, PEXA<0:15>, UP Stream	J41
PCIEX16	PCIE B1, PEXA<64:79>, Down Stream	J28
PCIEX16	PCIE B2, PEXB<80:95>, Down Stream	J26
PCIEX24	CPU Board connector ,for fabric mode	J48

4.4: LAN

Features	Description	Remark	
LAN1	Vendor	ASPEED	
	LAN Controller	AST2500	U134
	Transfers rate	10/100/1000Mb/s	

4.5: External I/O

Features	Description	Remark	
External I/O	1000M RJ45 with 1port	X1	J56
	Power Button	X1	SW2
	UID Button	X1	SW1
	BMC Reset	X1	J123

4.6: Internal I/O

Features	Description (type, Q'ty)	Remark
PEX9797 EEPROM Socket	For Switch FW, x3	J44/J22/J21

PEX9797 I2C Connector	For swtich debug, x1	J33
PEX8608 I2C Connector	For 8608 debug, x1	J34
CPLD JTAG	For CPLD FW, x1	J63
GPU Connector	Two connector for one GPU, x16	J1/J2,J3/J4,J5/J6, J7/J8,J9/J10,J11/J12/ J13/J14,J15/J16
GPU JTAG	X8	J17-J20/J23/J31/J25/J24
BMC FLASH Socket	For BMC FLASH, x1	J27
RTC Battery Socket	Battery, x1	J73
IPMB Connector	For IPMB, x1	J70
Power Connector	For Power, x9	J58-J62, J64-J67

4.7: Onboard header

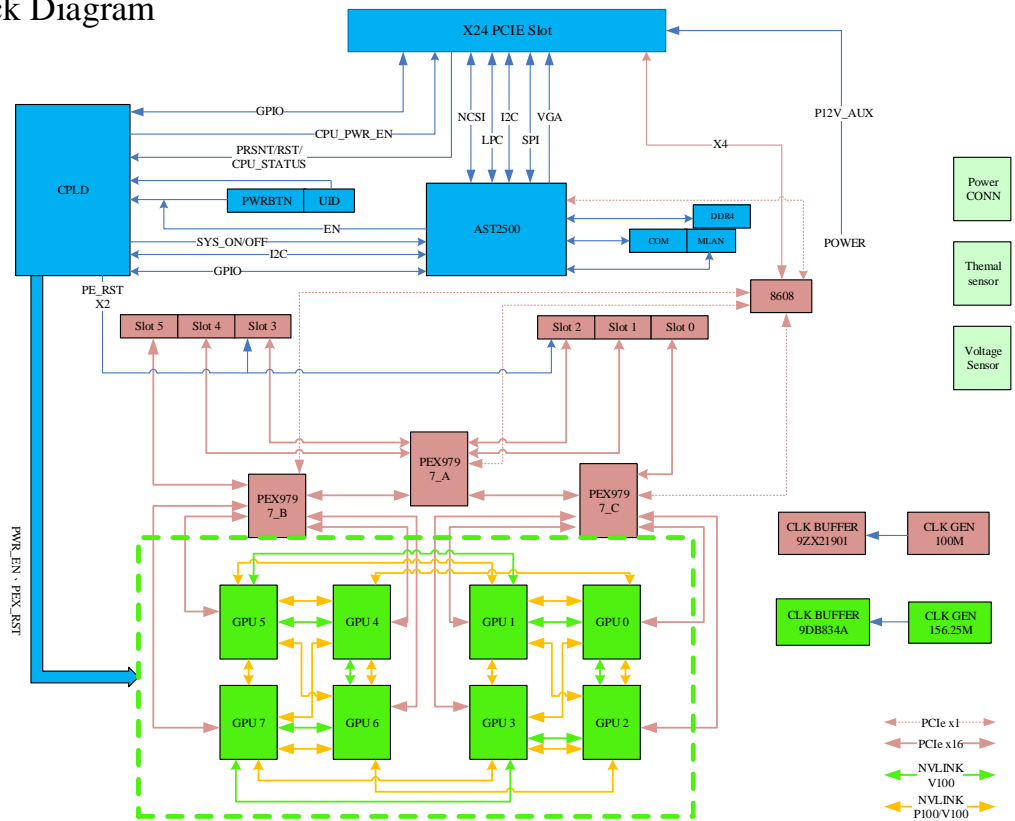
Features		Description(Q'ty)	Remark
On-board header	Fabric select	X3	J37/J35/J32(x3)
	VS/Base Mode select	X1	J51(x3)
	MCU0/1 JTAG	Flash the MCU FW, x2	J50/J47(x5)
	MCU0/1 UART	For MCU debug, x2	J46/J45(x3)
	BMC Reload	X1	J98(x3)
	Phy disable	X1	J125(x3)
	Sharelink disable	X1	J126(x3)
	Video disable	X1	J91(x3)
	BMC Uart	X1	J104(x4)
	SYS Uart	X1	J53(x4)
	1278 I2C header	X1	J38(x3)
	9797 VR I2C header	X1	J36(x3)

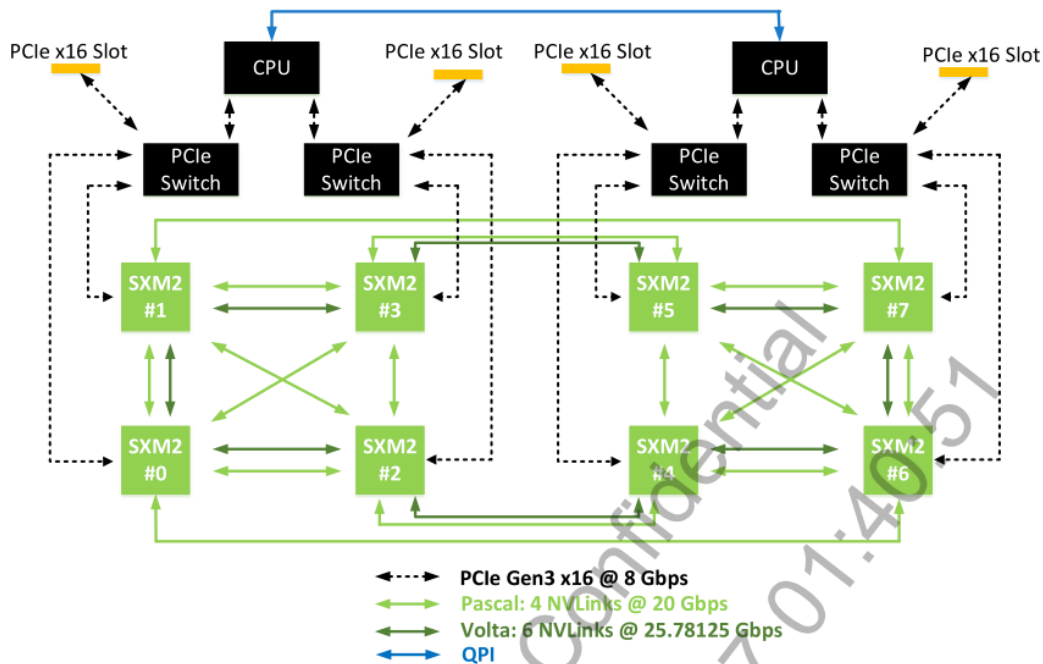
5: Architecture Block Diagram

5.1: MB block diagram

The GPU board user 3 PEX9797s for PCIE fan out and PCIE management. It has 8 SXM2 GPUs mounted under the switch. It also use BMC for board management and PEX8608 for fabric usage. Its block diagram is as follows.

GPU Block Diagram





- PEX9797 x3, for PCIE fan out
- PEX8608 for PCIE management signal router
- SXM2 GPU is the PCIE device
- The MCU manages GPU power and sideband signals.
- The CPLD controls power on/off
- AST2500 for Box management
- 1 X24 GEN3 PCIE slot for management CPU board
- 2 x16 GEN3 PCIE slot for upstream to host
- 4 x16 GEN3 PCIE slot for downstream to endpoint
- 1 management LAN from BMC for box management
- 1 external uart for BMC debug
- 1 external uart for CPU debug

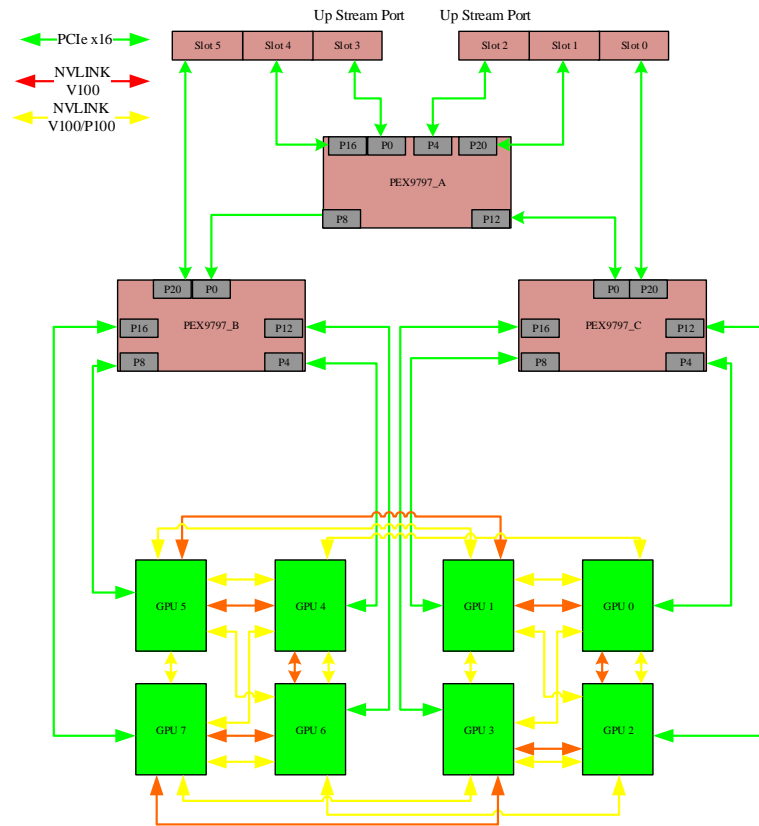
5.2: Chipset support

5.2.1 PEX9797 & GPU chipset:

PEX9797 is 96 lanes PCIE 3.0 PCIE switch. It has fanout mode and fabric mode. Fanout mode is the transparent bridge for host and endpoint. Fabric mode provide some advanced features such as PCIE management and Endpoint allocation etc,

In this GPU box, all of the three switches are configured as 6 x16 ports. The 9797_A port P0 and P4 are for upstream, others are for downstream.

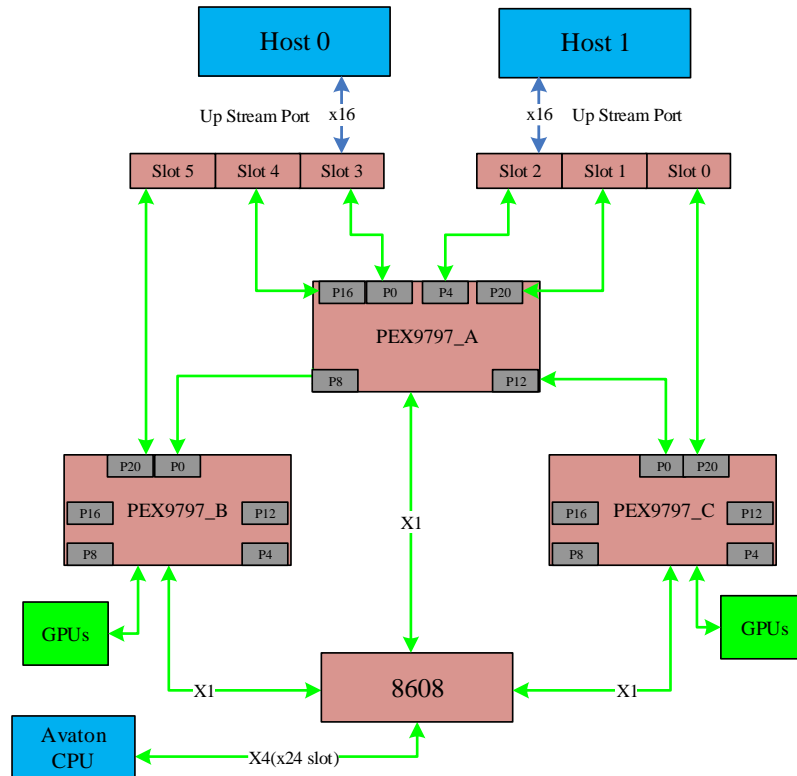
The 8 GPUs are PCIe endpoints by PCIe x16 port. In the GPU box, the NVLink topology compatible with SXM2 V100 and P100.



PCIe & NVLink topology

5.2.2 PEX9797 fabric mode

Fabric mode is for advanced research, the mode could support such as dual hosts , management PCIe endpoint and allocate endpoints from one to another. PEX9797 use the PCIe lane96 to connect management CPU(Avaton C2350, CPU Board) for the feature. For example, we can decide which gpu belongs to host0, and then change it to host1. The Avaton CPU is the management CPU for PEX9797, the management signal is route to PEX8608 first.

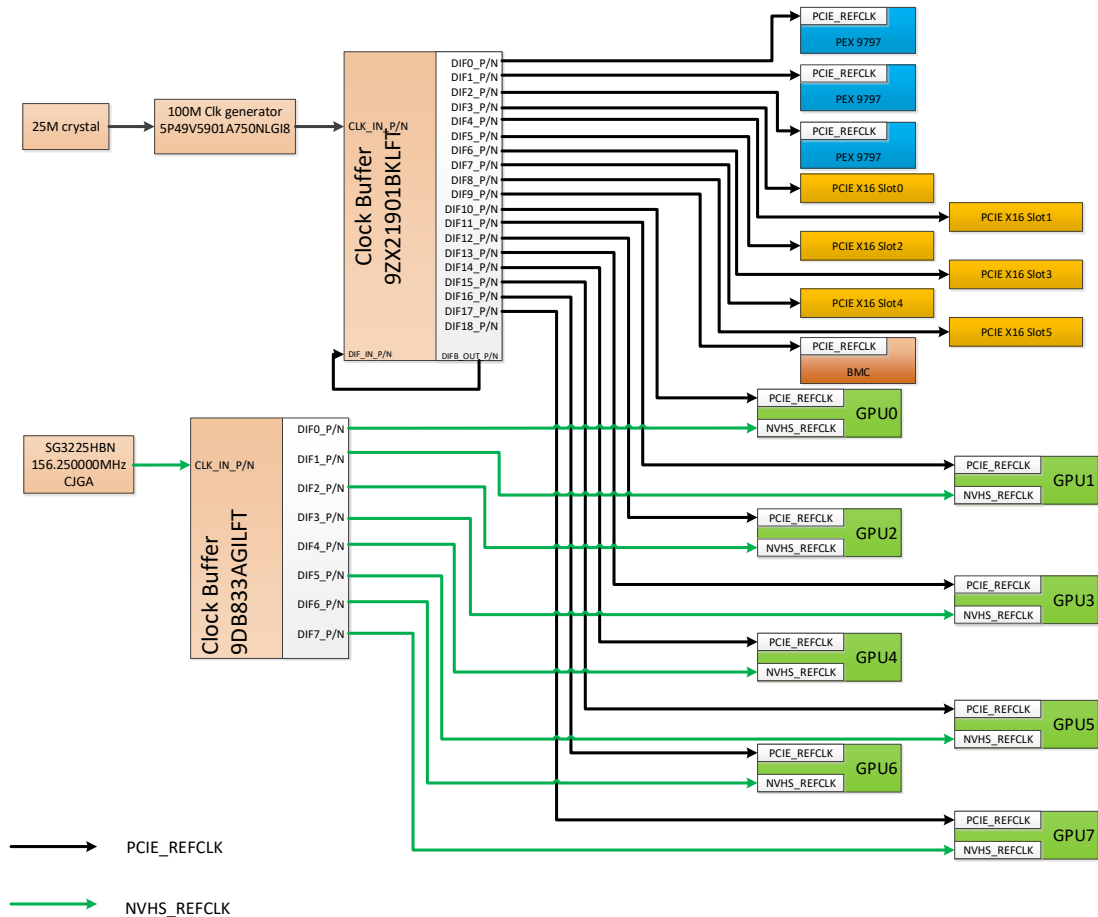


Fabric mode diagram

5.3 Clocking

The system use cfc clock generated local. All the PCIE switch and PCIE endpoint clocks come from the same clock buffer. The diagram as follows.

- 18X 100MHZ for PCIE
- 8X 156MHZ for GPU NVLink



5.4: On Board Slot

Refer to 1.5 for details.

5.5: BMC

- ASPEED AST2500 chip with 4Gb DRAM
- Embedded NIC dedicated for management, 100/1000 Mbps port
- 1 COM ports support
- Embedded video (VGA) with 16MB video memory
- SMBUS 2.0 specification compliant
- Thermal sensor

5.6: I/O connector or onboard header

- 1 x1000M RJ45 connector for dedicated LAN



- 2 of 6 PCIe x16 slots for upstream, 4 ports for device.
- 1 x24 PCIe 3.0 slot for management cpu.
- 1 x6pin I2C header for 9797 debug
- 1 x5pin JTAG header for MCU FW
- 1 x10pin JTAG header for CPLD FW
- 1 x30 pin IPMB connector for BMC communication, IPMB bus based on I2C interface

6: Environmental Requirements

This section provides regulatory and compliance information applicable to this system.

6.1 Product Regulatory Compliance

Markings

This product shall be certified with the following Product Certification Markings for any deployments for their respective regions.

6.2 Operating environment

- | Operating temperature: 5°C to 40°C (41°F to 104°F)
- | Non-operating temperature: -40°C to 70°C (-40°F to 158°F)
- | Operating relative humidity: 20% to 85%RH
- | Non-operating relative humidity: 10% to 95%RH